

MODEL NAME :VAW03

PCB NO : LA-9103P

BOM P/N : DA60000UT00 LA-9103P M/B

DA40001FO00 LS-9101P POWER BUTTON/B

DA40001FP00 LS-9102P USB/B

DA40001FQ00 LS-9103P TP BUTTON/B

Inspiron Value OAK(Essentials) 15 UMA (Comal Richland)

Inspiron Value OAK(Essentials) 15 Discrete#1 (Comal Richland, AMD Mars Pro)

Inspiron MainStream OAK(Essentials) 15 UMA (Comal Richland)

Inspiron MainStream OAK(Essentials) 15 Discrete#2 (Comal Richland, AMD Mars Pro)

Vostro Value OAK(Essentials) 15 UMA (Comal Richland)

Dell / Compal Confidential

Schematic Document

AMD FP2 Richland Processor with DDRIII + Bolton M3 FCH

AMD VGA Sun XT

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

UMA@ : Only for UMA

DIS@ : Only for Discrete

GCLK@ : Green CLK implemented

NGCLK@ : Non Green CLK implemented

@3221: ALC 3221

@3223 : ALC 3223

EMC@ : EMC Parts

2nd@ : for APL3512 2nd source control

(RN9, RV32, RL22)

2012-11-26

Rev: 0.2

R1@ : R1 P/N for PCB

R3@ : R3 P/N for PCB

THR1@ : Thames-XT R1 P/N

THR3@ : Thames-XT R3 P/N

CHR1@ : Chelsea-Pro R1 P/N

CHR3@ : Chelsea-Pro R3 P/N

R@ : RTD2132-R

S@ : RTD2132-S

X76@ : VRAM Group

CH@ : Chelsea M2

SE@ : Seymour M2

TH@ : Thames-XT

Mars@ : Mars Pro M2

A4R1@ : A4 APU-R1

A6R1@ : A6 APU-R1

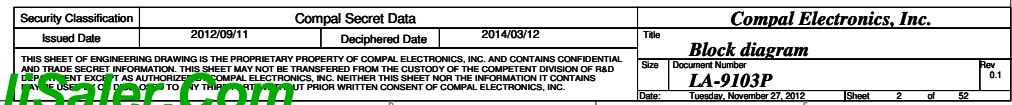
A8R1@ : A8 APU-R1

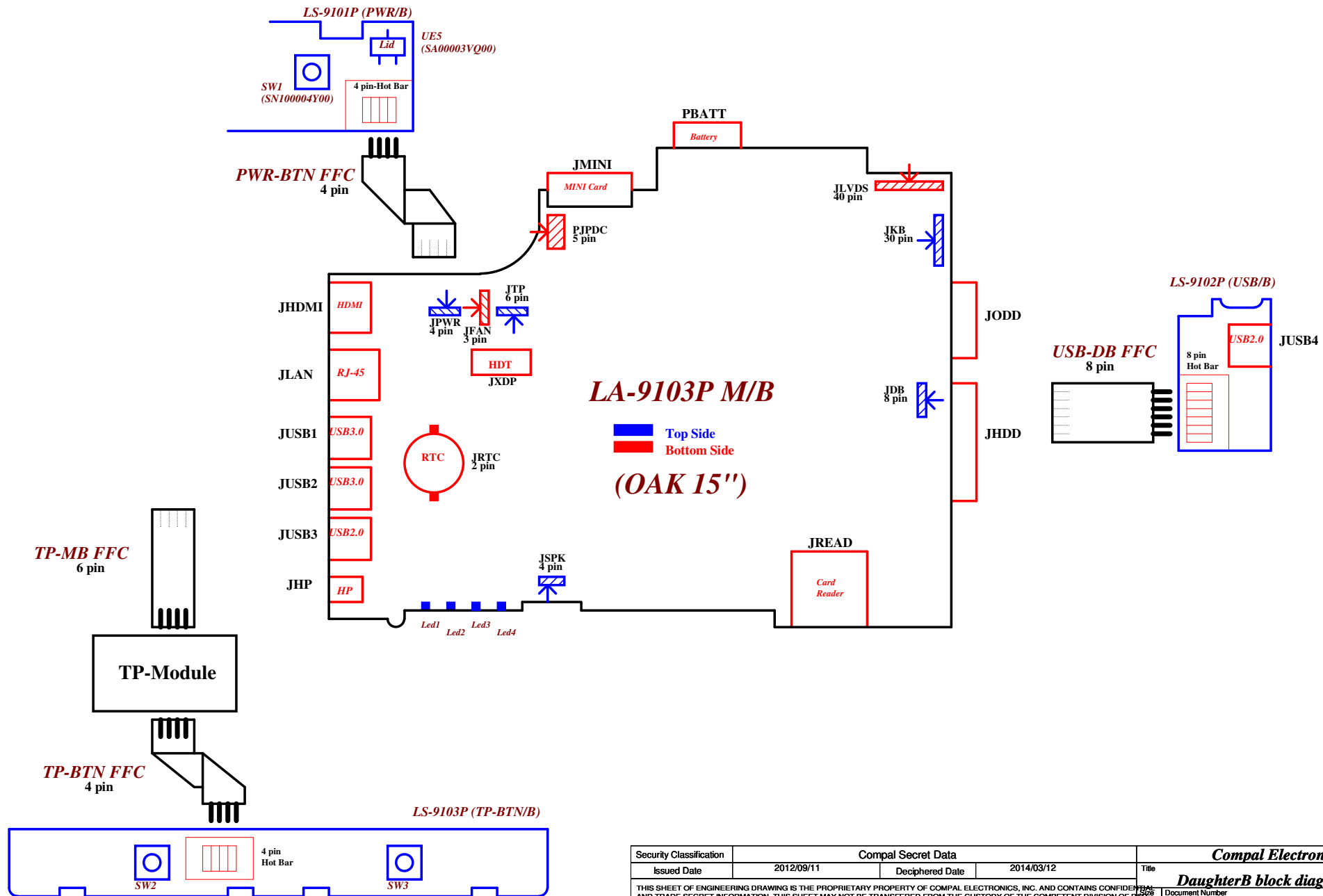
A8@ : A8 APU Symbol

Hud@ : HUDSON-M3

Bol@ : BOLTON-M3

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				Date	Tuesday, November 27, 2012
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				Rev	0.1





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Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	000 1011	11h 0x16	ADM1032ARMZ	100 1101	4Dh 0x9A
Charger IC	000 1001	09h 0x12	SB-TSI	100 1100	4Ch 0x98
			RTD2132	100 1010	4Ah 0x94
			GPU	100 0001	41h 0x82

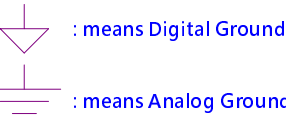
SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

Symbol Note :



FCH

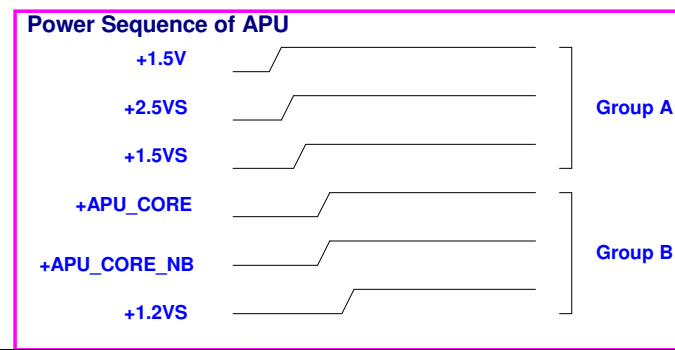
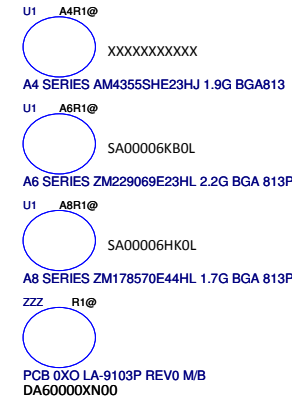
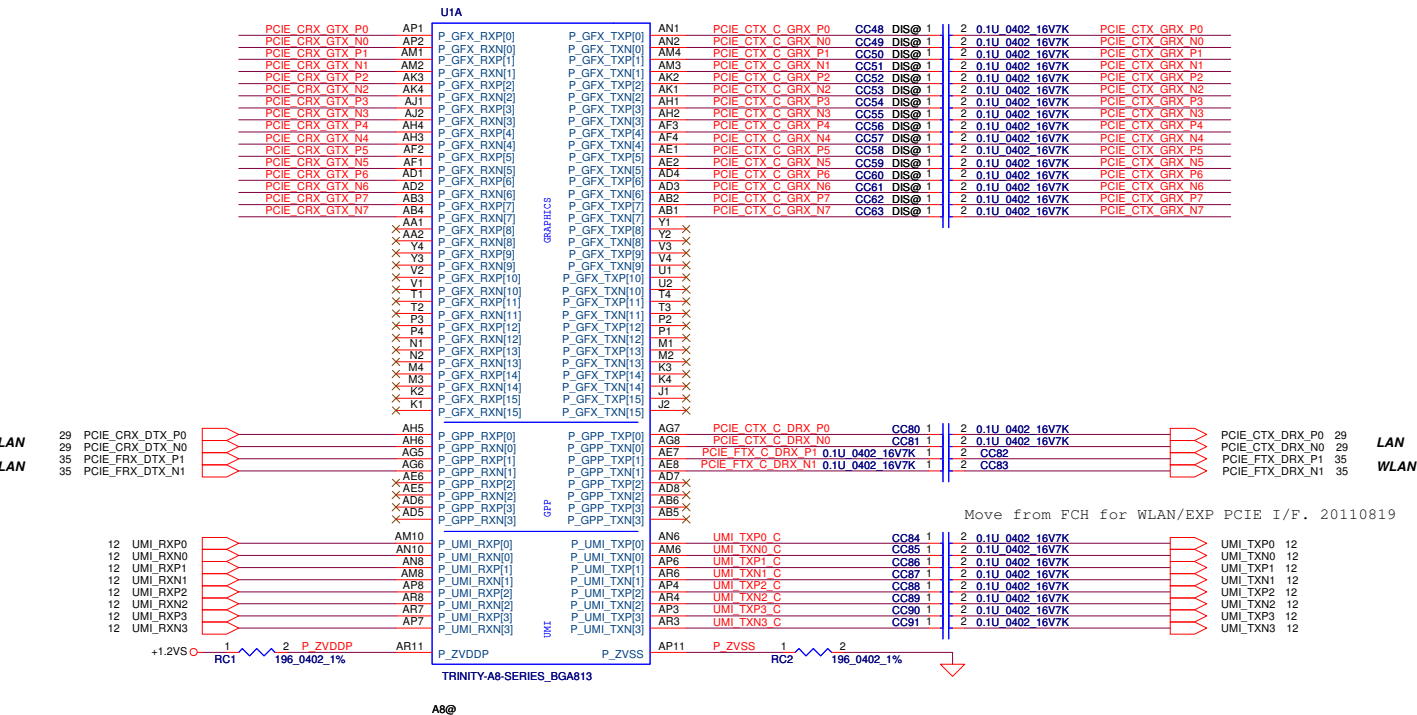
USB PORT#	DESTINATION
0	USB conn.3 DEBUG PORT
1	MINI CARD (WLAN)
2	USB conn.4
3	NC
4	NC
5	NC
6	Card Reader
7	NC
8	NC
9	Camera
10	USB conn.2
11	NC
12	NC
13	USB conn.1

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	None
	CLKOUT_PCIE1	None
	CLKOUT_PCIE2	10/100 LAN
	CLKOUT_PCIE3	MINI CARD WLAN
	CLKOUT_PCIE4	None
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	None
	CLKOUT_PEG_B	None

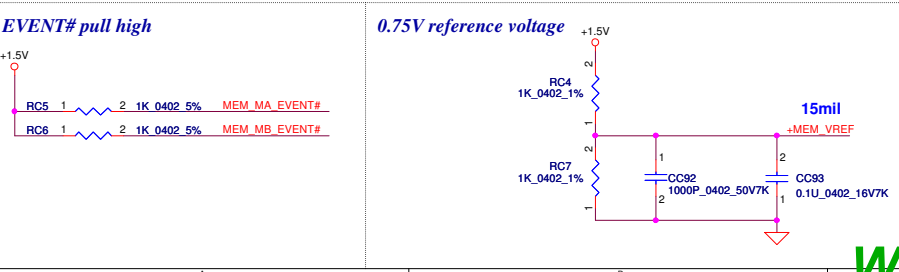
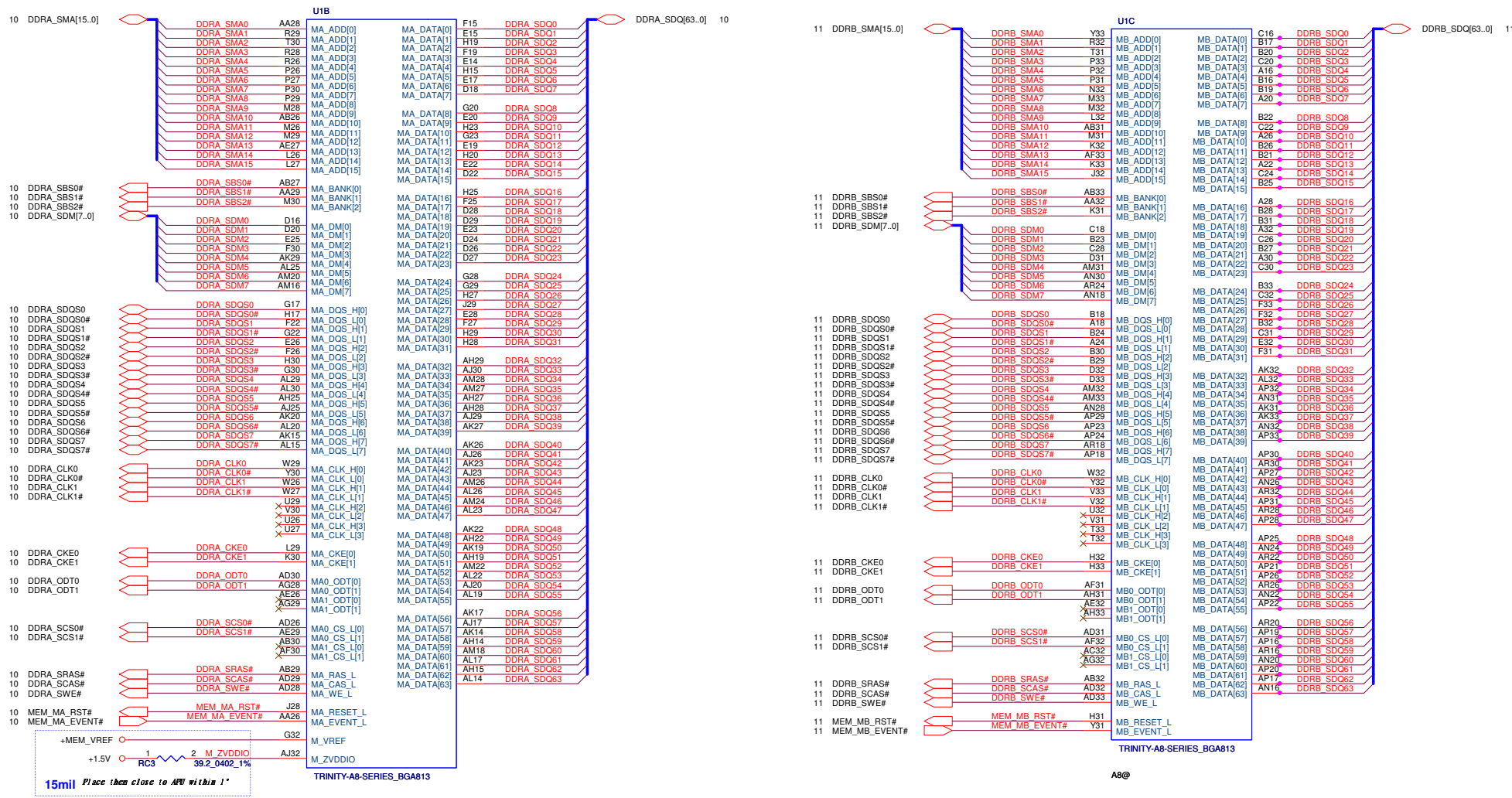
SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

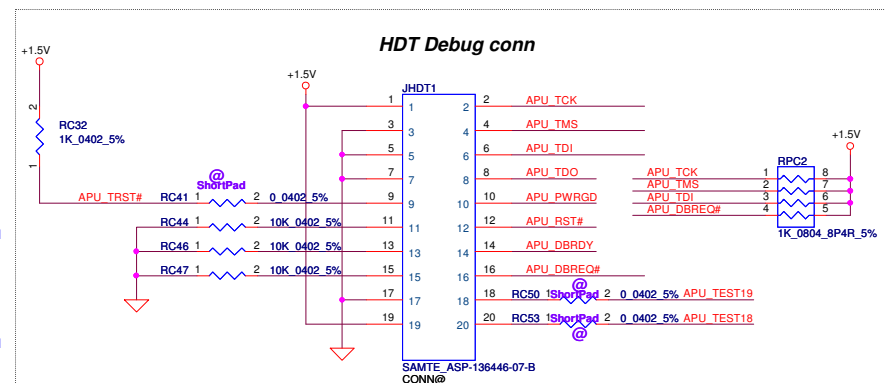
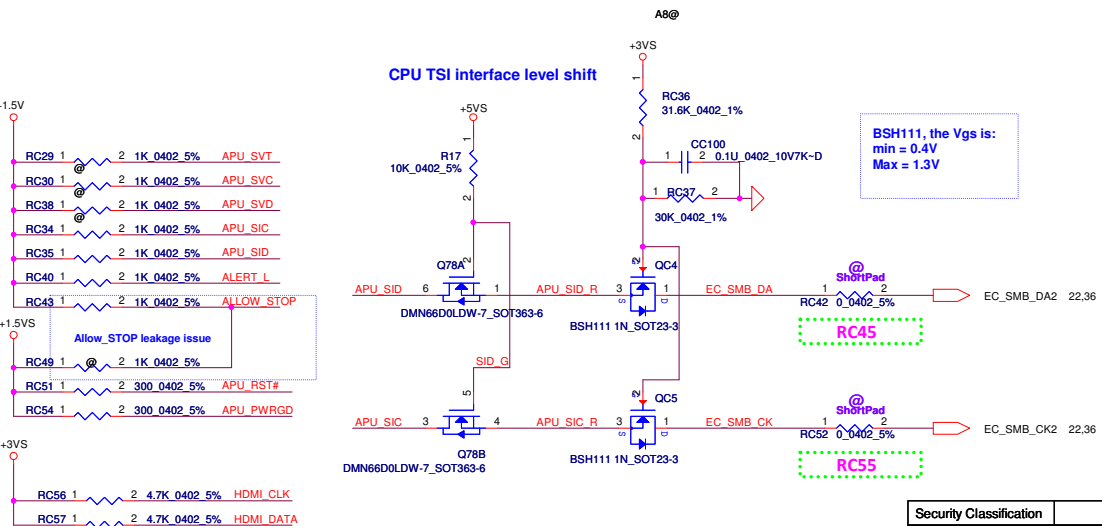
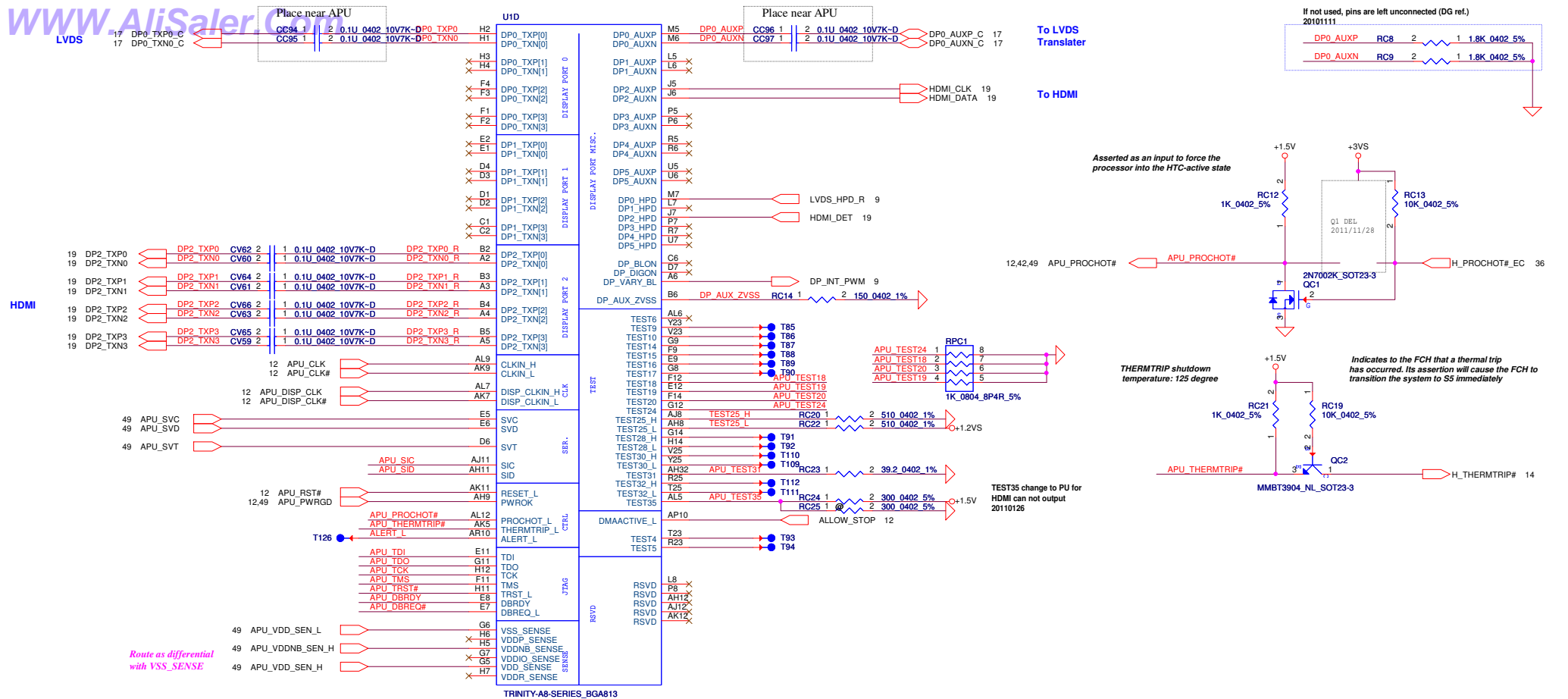
21 PCIE_CRX_GTX_P[0..7] 21
21 PCIE_CRX_GTX_N[0..7] 21



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Date				Tuesday, November 27, 2012				Rev			
Sheet				5				0.1			

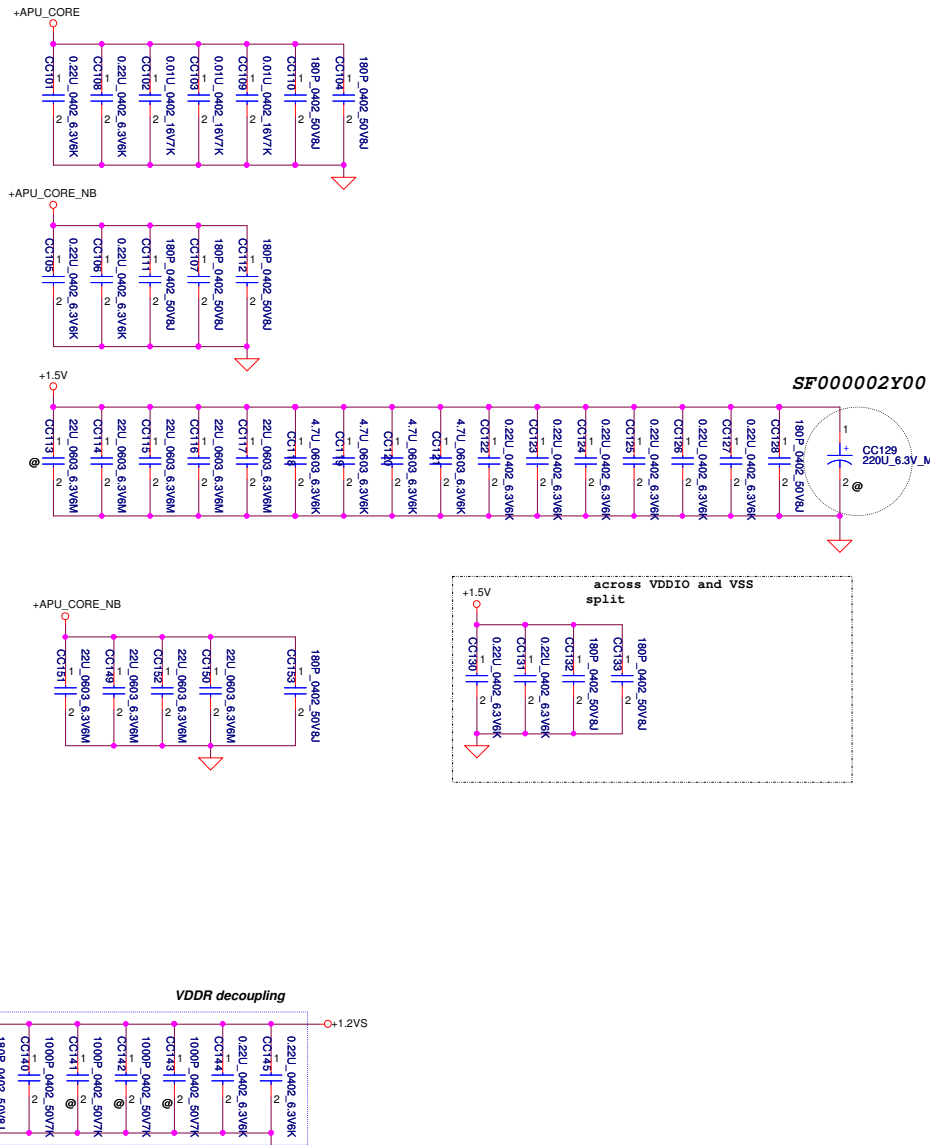


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	2012/09/11			FP2 DIII Memory I/F	LA-9103P		
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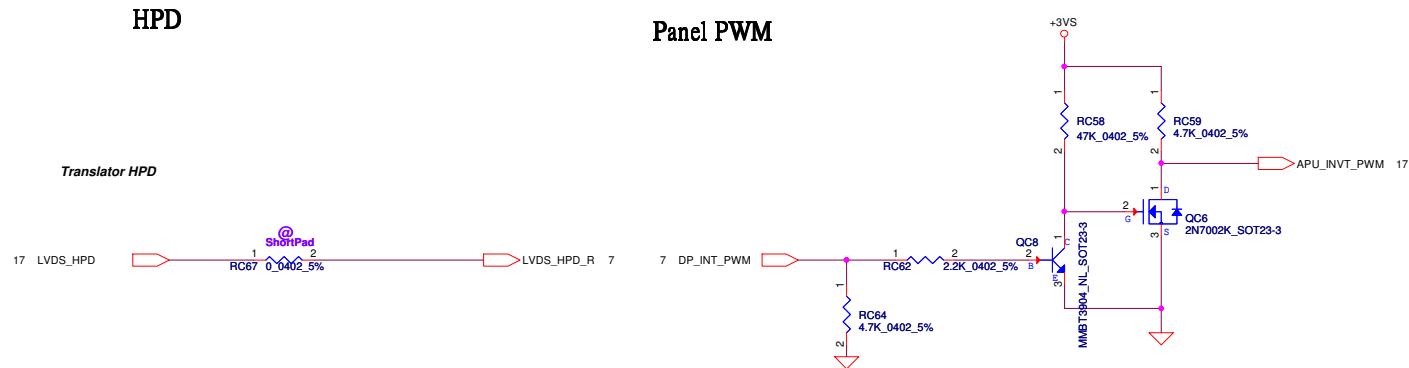
Power Name	Consumption
VDD	60A
APU CORE	

A8@

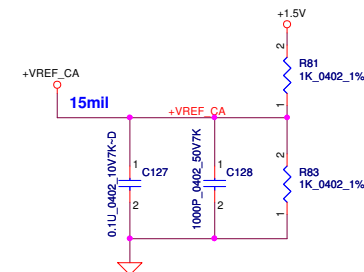
APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	0.01uF x 2
	180pF x 2	3.3nF x 1	10uF x 12

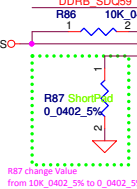
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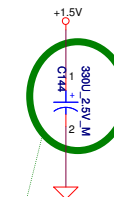
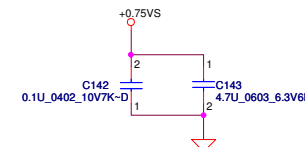
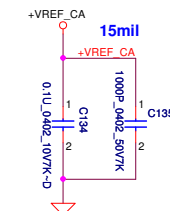
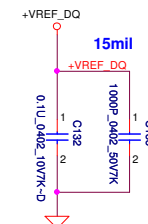
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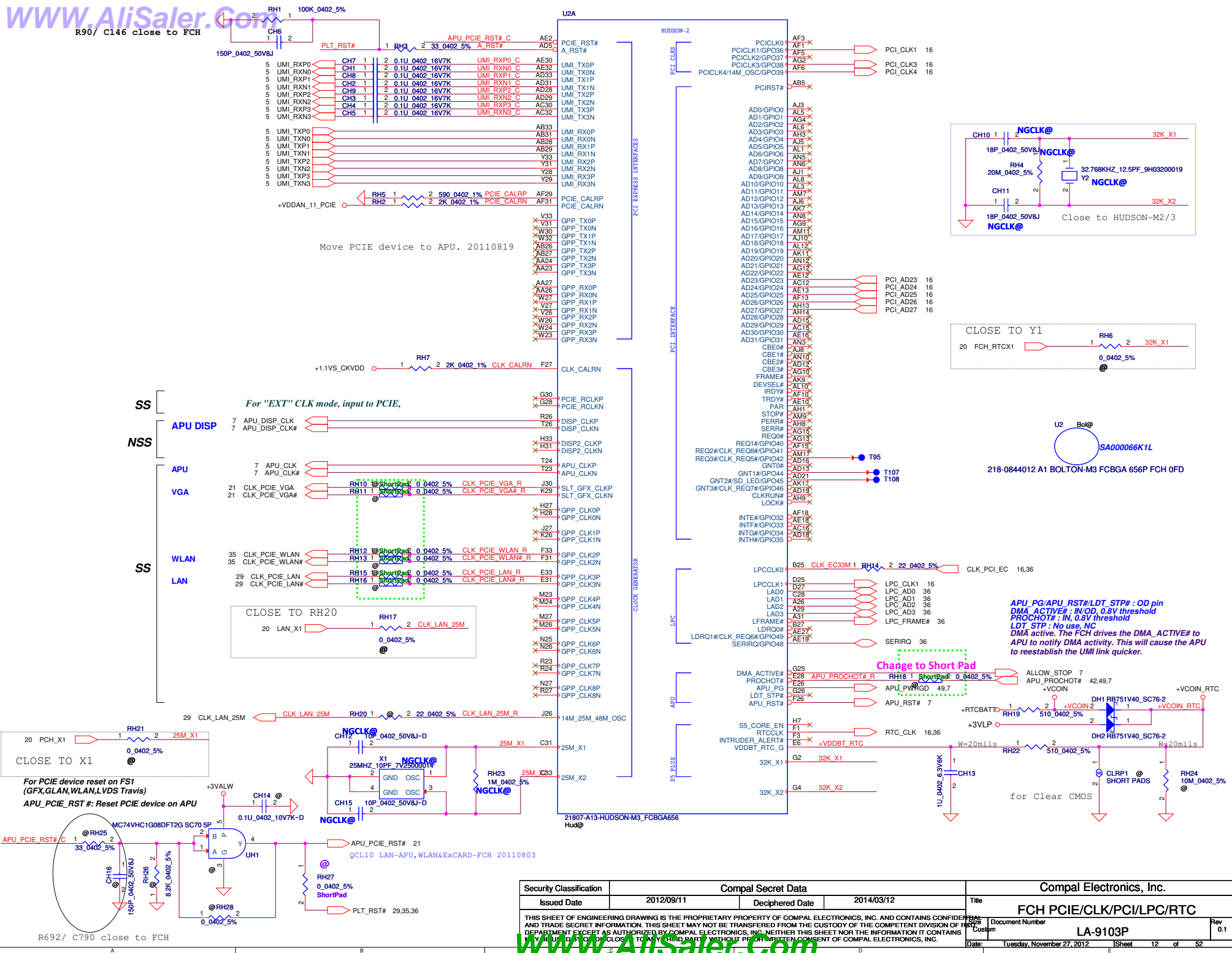
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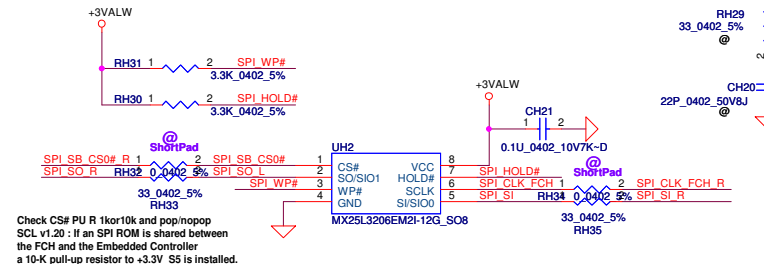
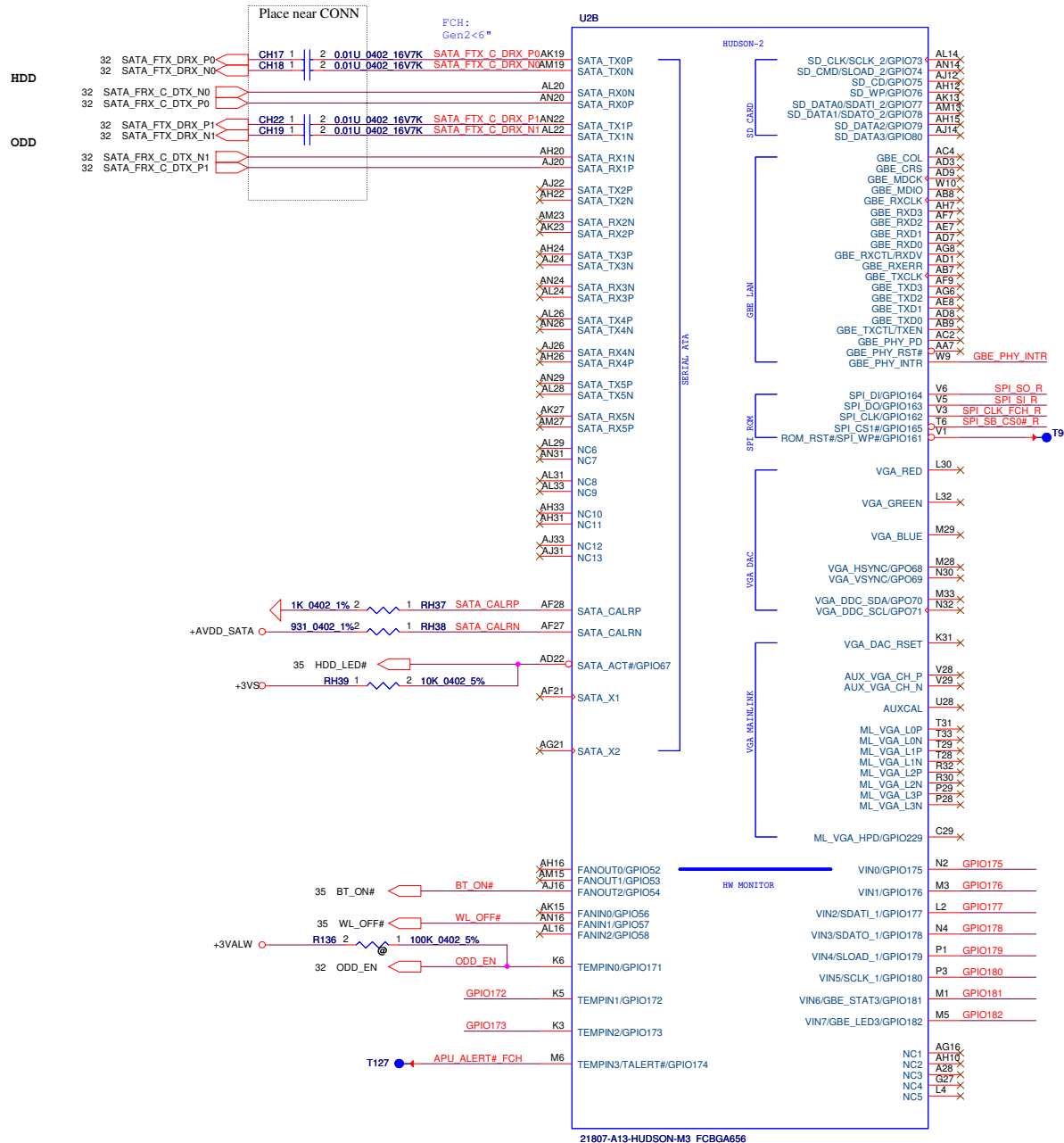
(330uF 6.3V 4.2L ESR17m) *1= (SF000002Z00)

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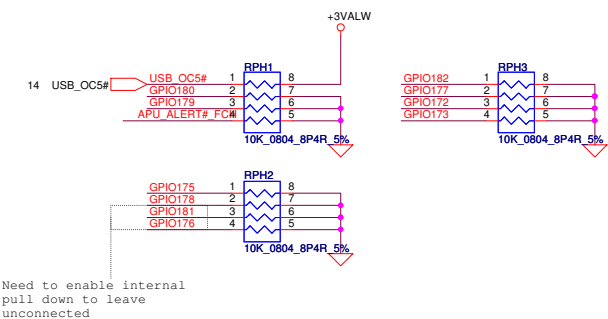


4MB SPI ROM & Non-share ROM.



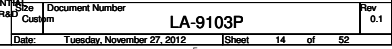
GBE_PHY_INTR
Pulled-up to +3.3V_S5 with a 10-K 5% resistor.
FCH SCL v1.20 #19-85

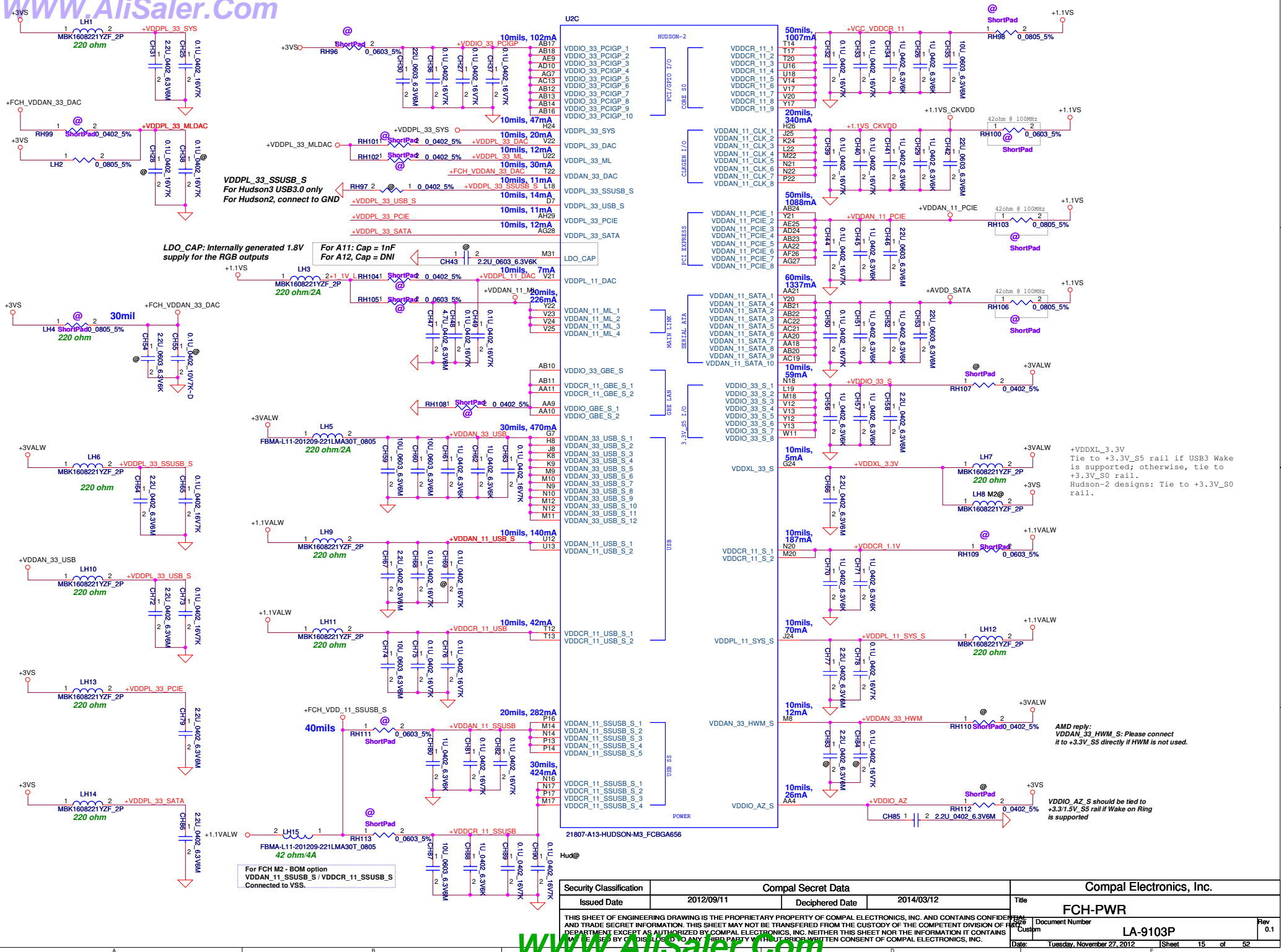
Removed RGMII/MII support and updated termination
requirements for GBE_COL, GBE_CRD, GBE_RXERR
and GBE_MDIO when RGMII/MII interface is not used.
FCH DGv1.20 / SCL v1.20



Hud@

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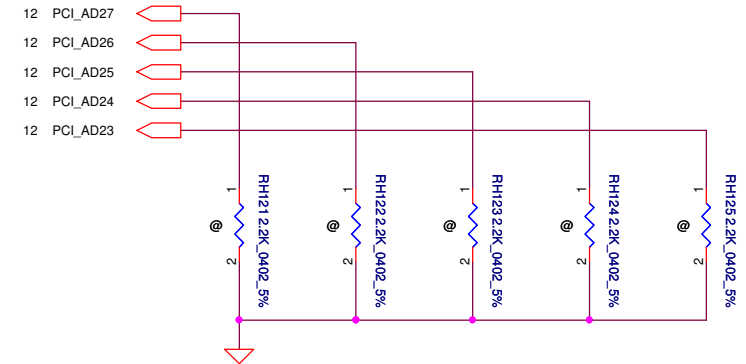
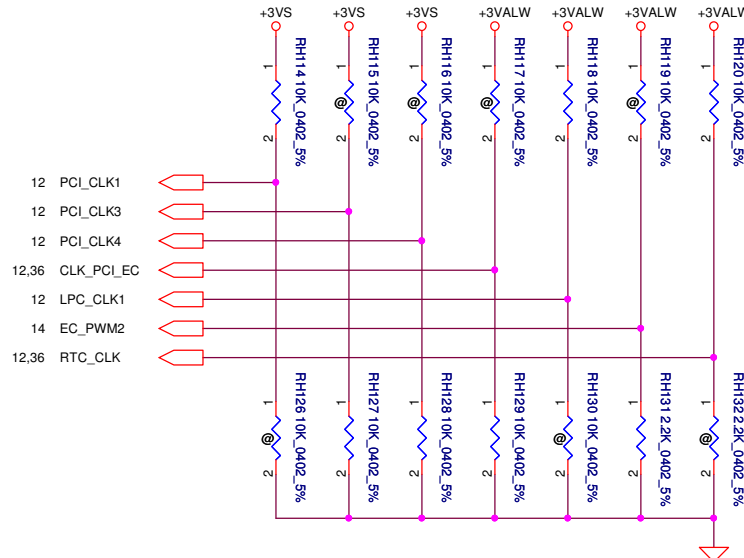
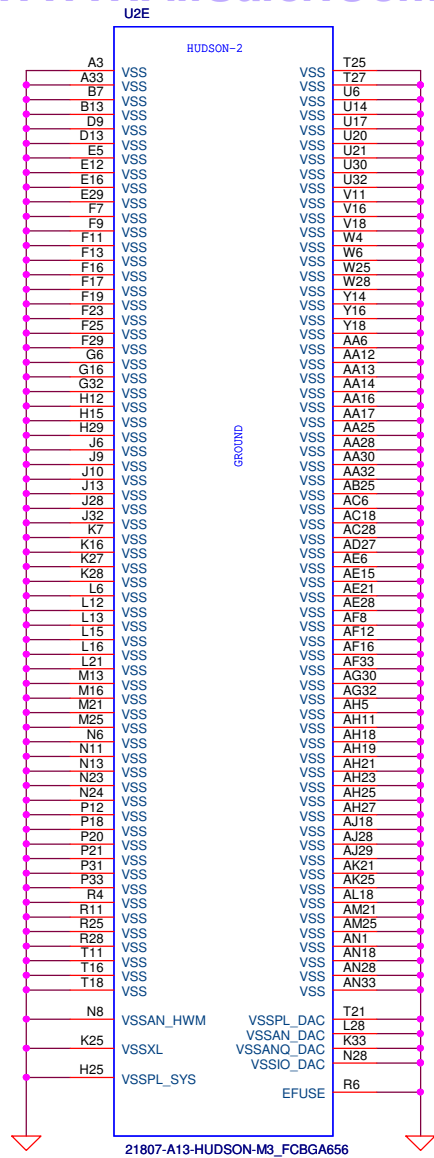
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

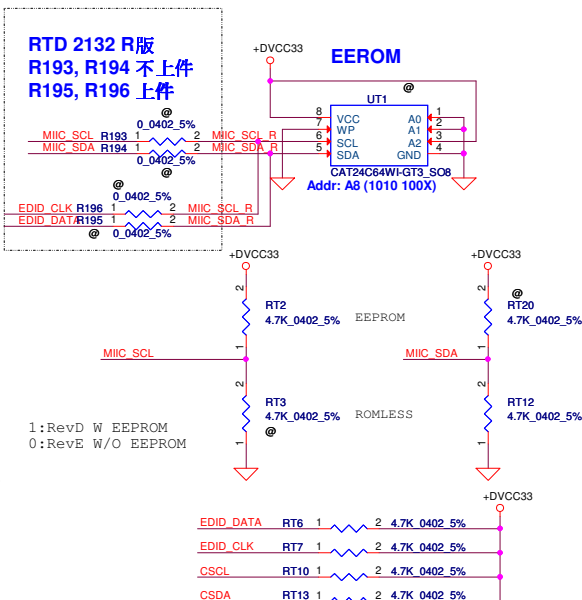
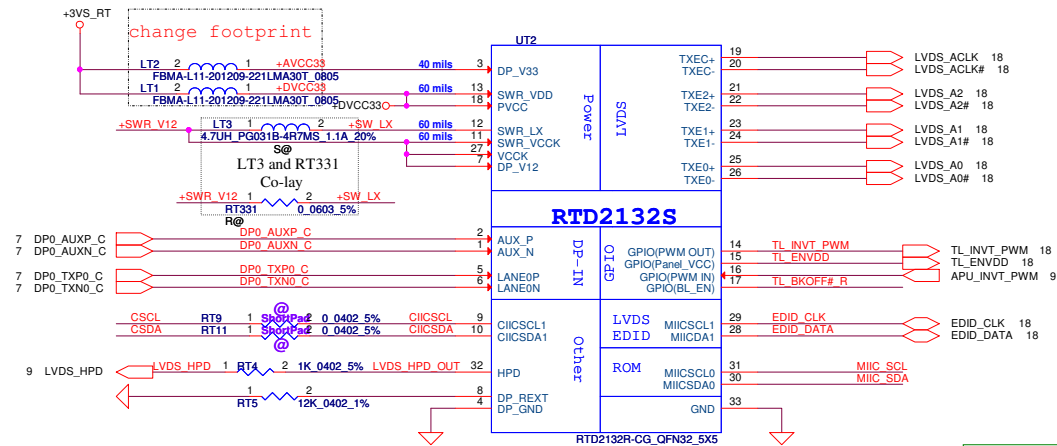
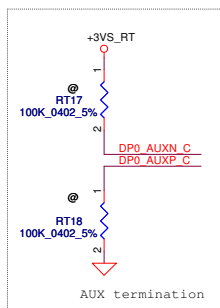
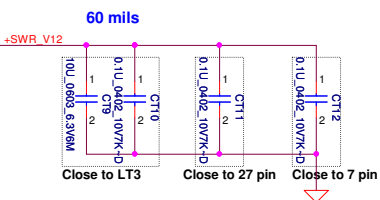
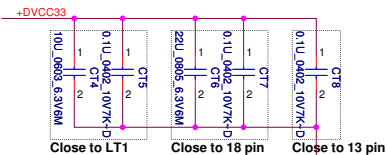
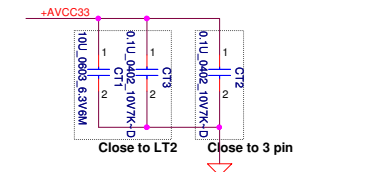
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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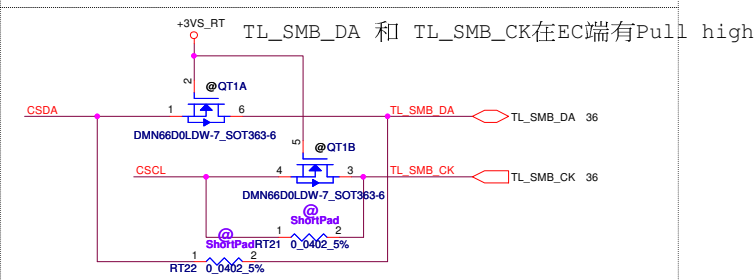
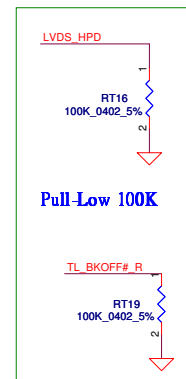
Power Consumption:

Pin3 (DPV33) < 20mA
 Pin 7 (DP_V12) < 100mA
 Pin 11 (SWR_VCCCK) < 100mA (layout trace > 60 mil)
 Pin 12 (SWR_LX) < 600mA (layout trace > 60 mil)
 Pin 13 (SWR_VDD) < 200mA (layout trace > 40 mil)
 Pin 18 (PVCC) < 50 mA
 Pin 27 (VCCCK) < 50mA



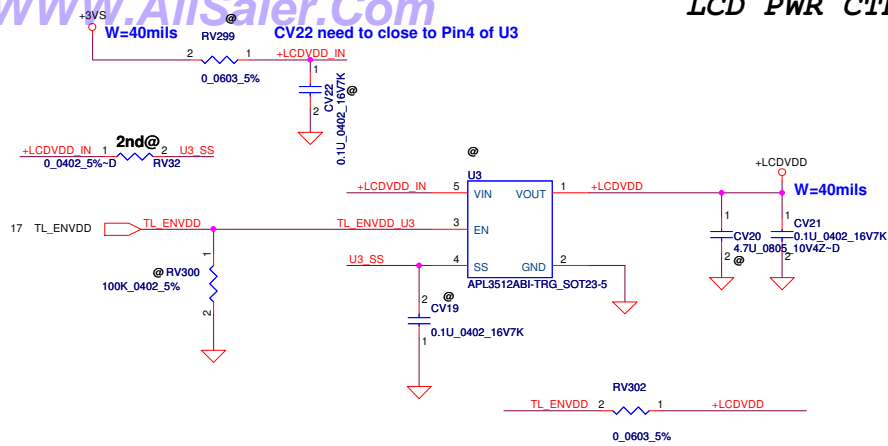
		Pin30	
		0	1
Pin31	0	x	EP MODE
	1	ROM	EEPROM

Vendor advise reserve it

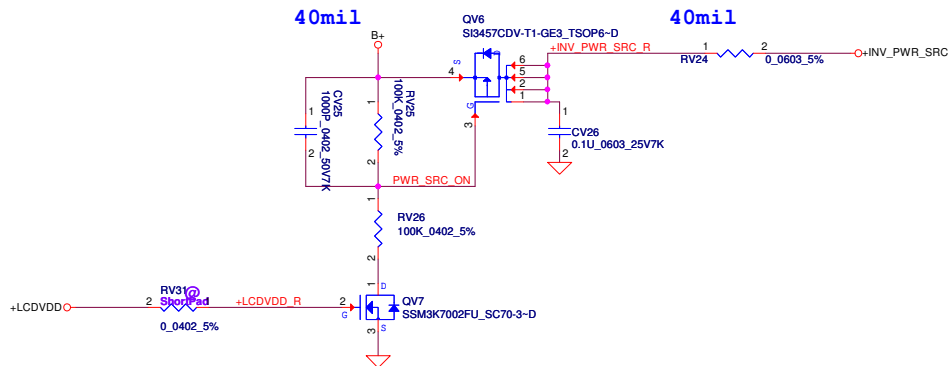


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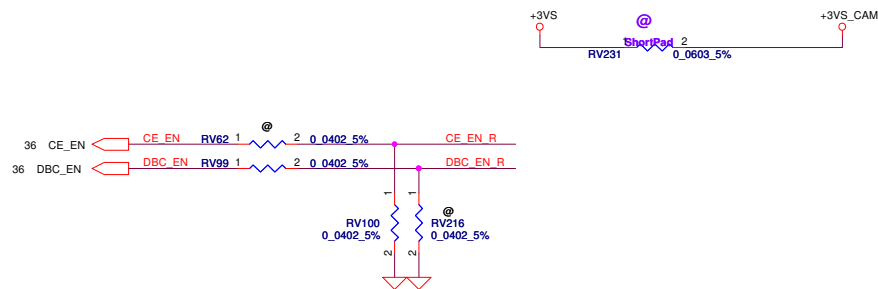
LCD PWR CTRL



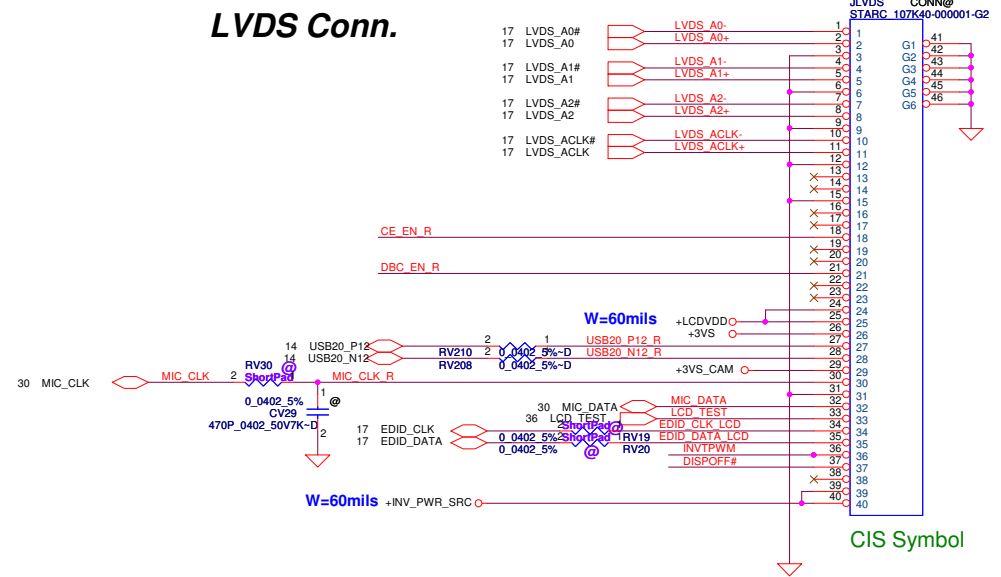
LCD backlight PWR CTRL



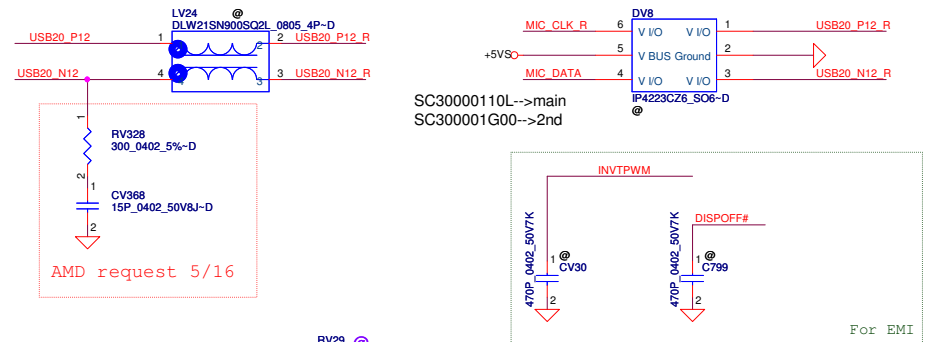
Wedcam PWR CTRL



LVDS Conn.

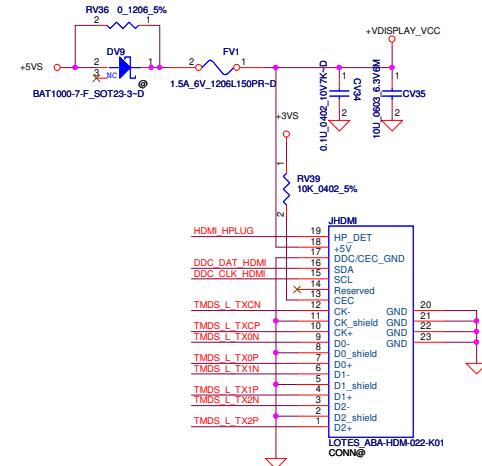
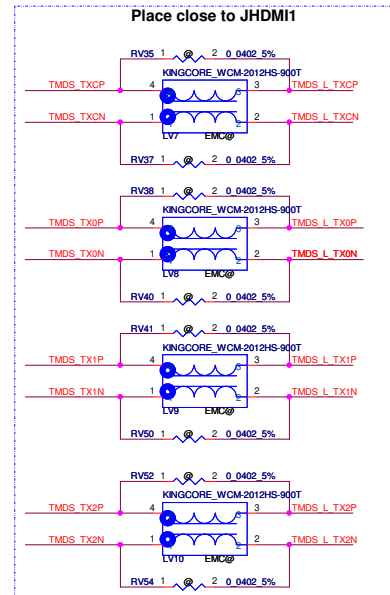
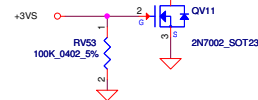
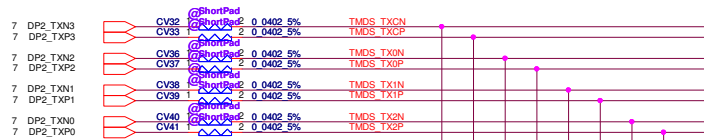


* Reserved for EMI/ESD/RF
need to close to JLVDS

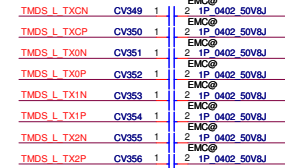
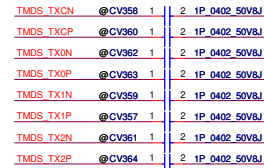


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				Date	Sheet
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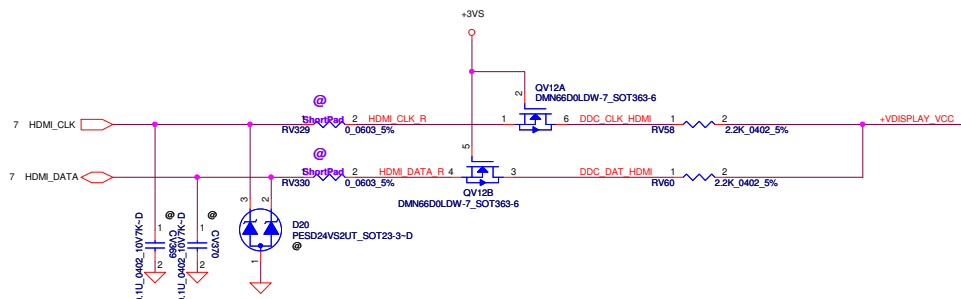
W=40mils



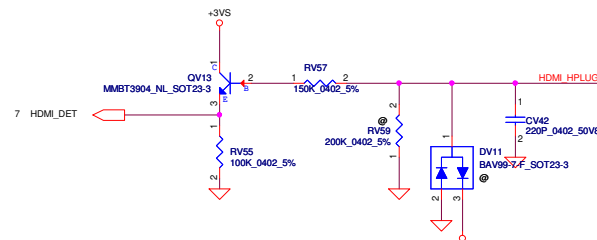
Part Number	Description
R0000000023M	HDMI W/Logo:R0000000023M

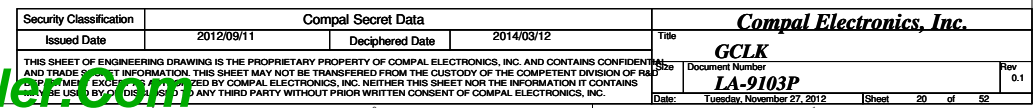


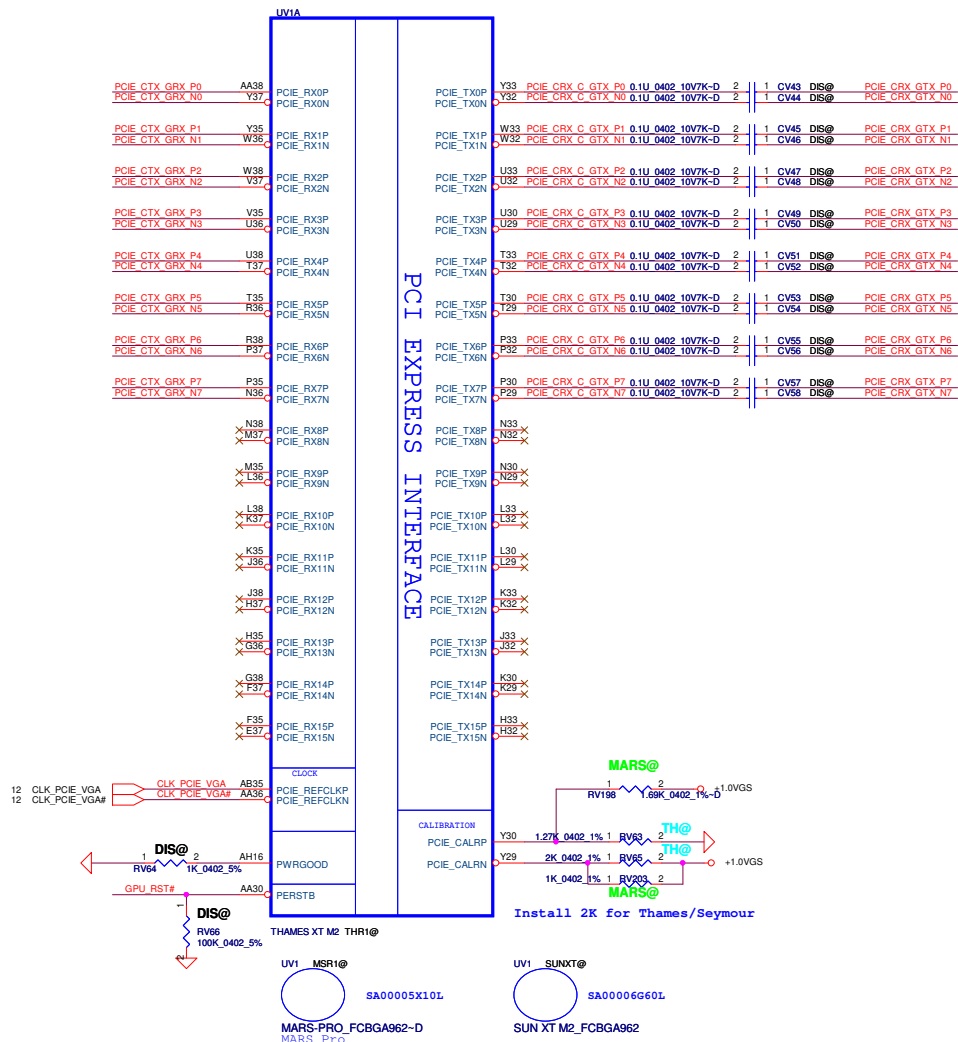
20121127 EMI ADD



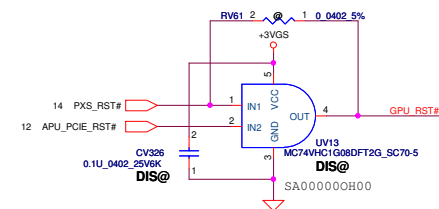
CV365, CV367
Please close APU side







UViG		
LVDS CONTROL	VARY BL DIGON	AK27 AJ27
		AK35 AK38
TXCLK_LP_DPFP3P	TXCLK_UN_DPFP3N	AJ38 AK37
TXOUT_U0P_DPFP2P	TXOUT_U0N_DPFP2N	AK35 AK38
TXOUT_U1P_DPFP1P	TXOUT_U1N_DPFP1N	AK35 AK38
TXOUT_U2P_DPFP0P	TXOUT_U2N_DPFP0N	AK38 AK37
TXOUT_U3P	TXOUT_U3N	AK35 AK38
LVTMPD		AP34 AP33
TXCLK_LP_DPFP3P	TXCLK_LN_DPFP3N	AJ38 AK37
TXOUT_L0P_DPFP2P	TXOUT_L0N_DPFP2N	AK37 AK38
TXOUT_L1P_DPFP1P	TXOUT_L1N_DPFP1N	AK37 AK38
TXOUT_L2P_DPFP0P	TXOUT_L2N_DPFP0N	AP35 AK38
TXOUT_L3P	TXOUT_L3N	AK36 AP37



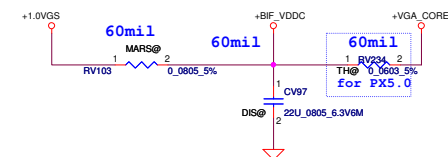
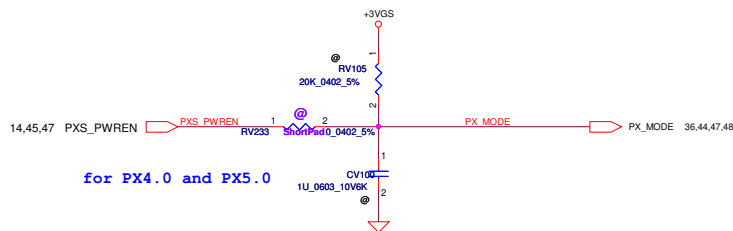
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	ATI ThamesXT M2 PCIE/LVDS
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PX_MODE=1 for Normal Operation

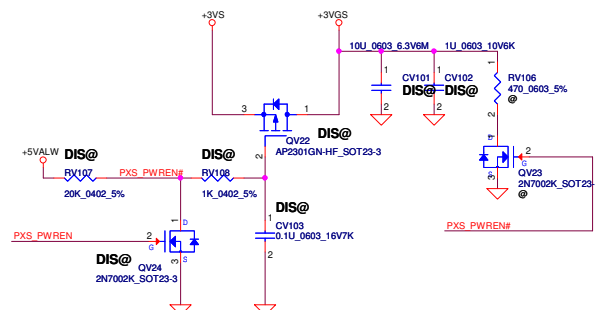
PX_MODE=0 for BACO mode to shut down power rails except VDDR3, PCIE_VDDC and 1.8V rail

Switch circuits in BACO desings for Thanos/Seymour only

55mA@1.0V, in BACO mode



+3.3VS TO +3.3VGS



+1.5VGPU TO +1.5VGS



+1.5VGPU直接由Power網路Control

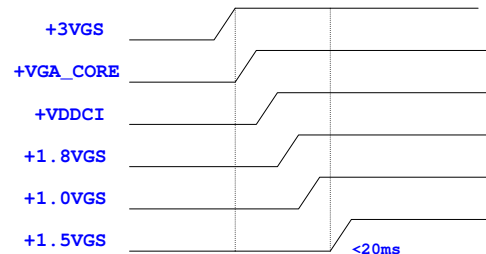
Note:

PX4.0 +VGA_CORE, VDDCI, +1.5VGS OFF

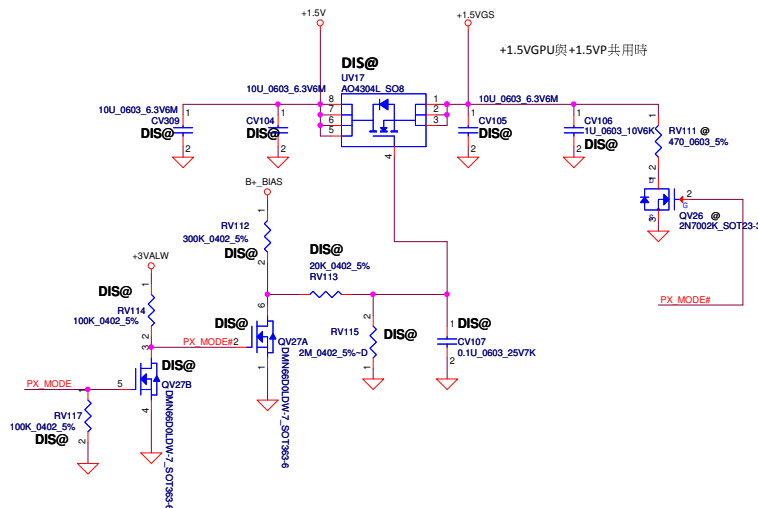
PX4.0 +3VGS, +1.0VGS, +1.8VGS ON

PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF

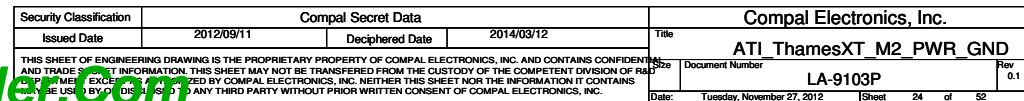
Power Sequence of Thames and Chelsea

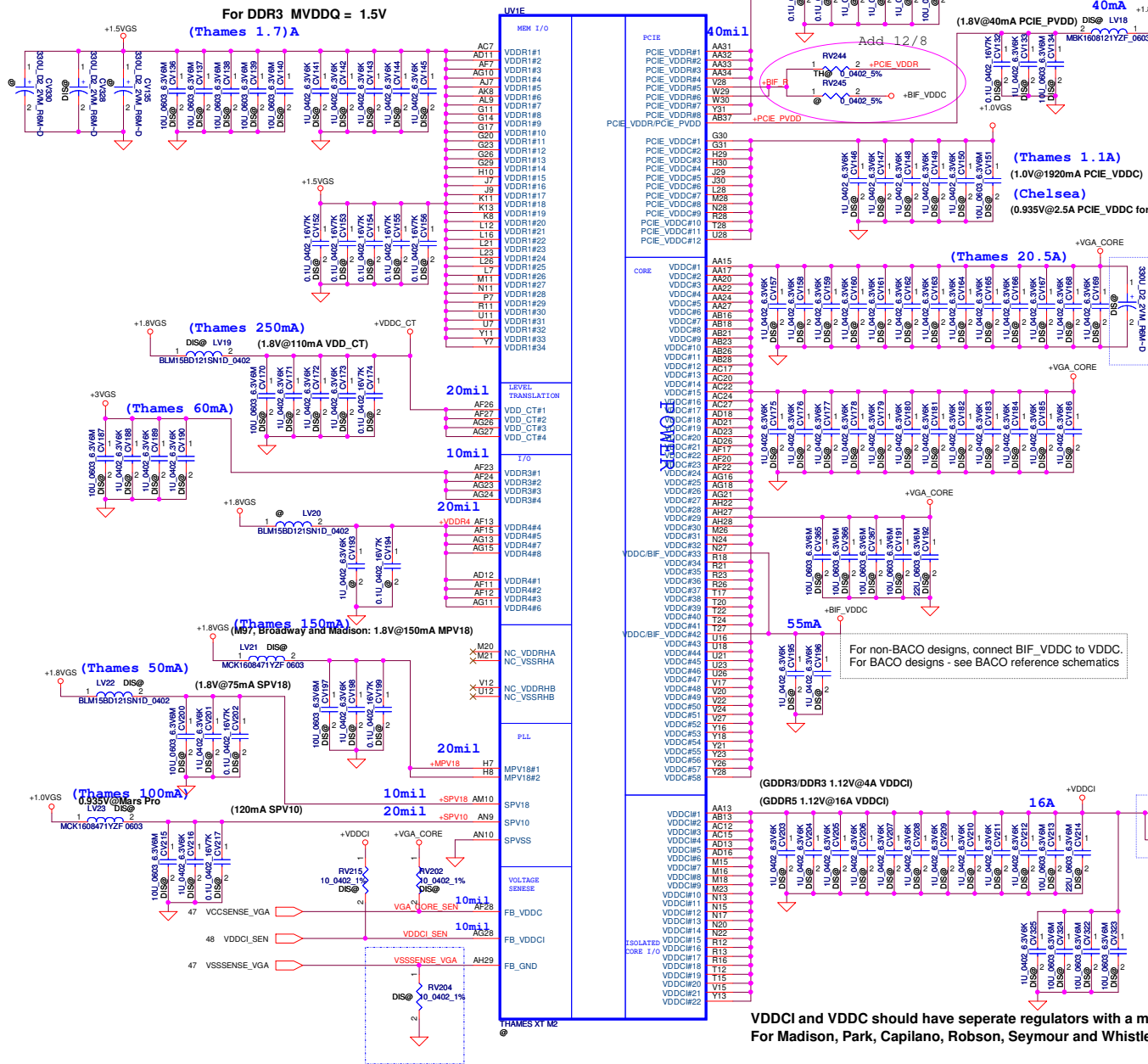


+1.5V TO +1.5VGS



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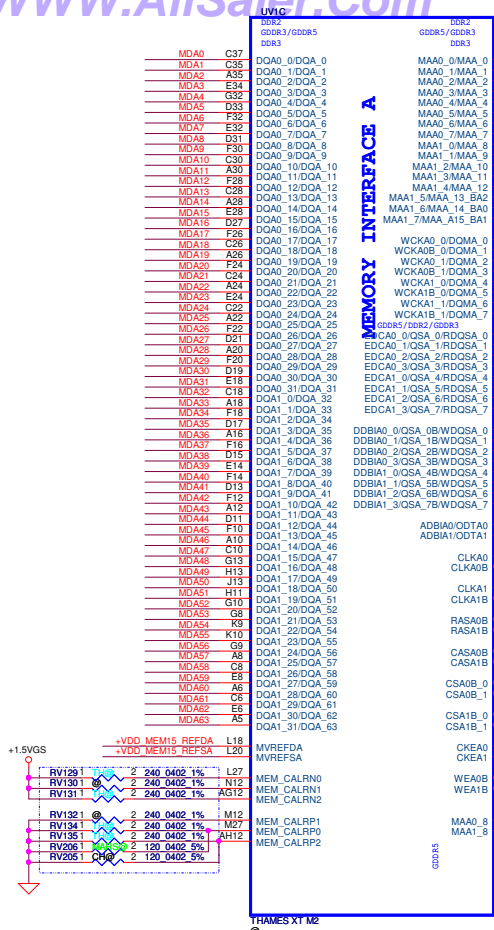
For Thames/Seymour
BIF_VDDC is connected to VDDC in non BACO designs
BACO designs, switch circuits is required so that
when GPU is operating, BIF_VDDC is connected to VDDC,
while in BACO mode, BIF_VDDC is connected to +1.0V

For MARS/VENUS/HEATHROW/CHELSEA
BIF_VDDC should be connected with 0.95V

On Heathrow/Chelsea/Venus/Mars only
PCIE_VDDC : 0.95V @ 1.3A (GEN3.0)

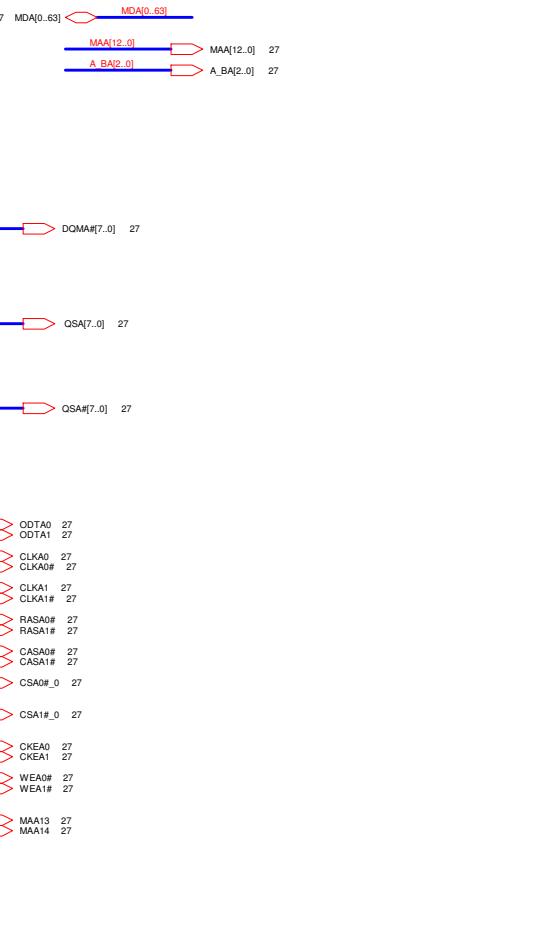
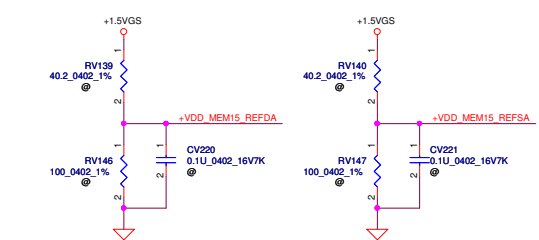
VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

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Issued Date	2012/09/11	Deciphered Date	2014/03/12	AT1 ThamesXT M2 Power	
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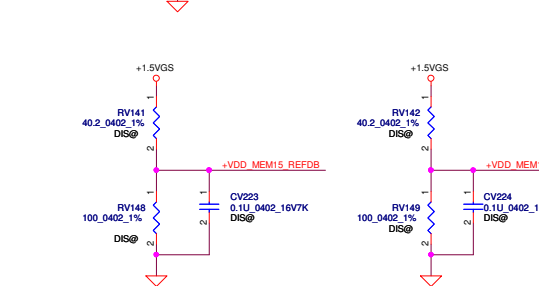
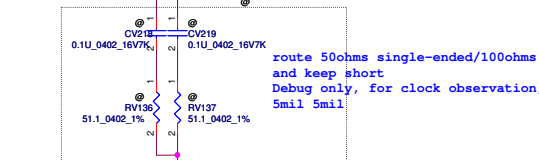
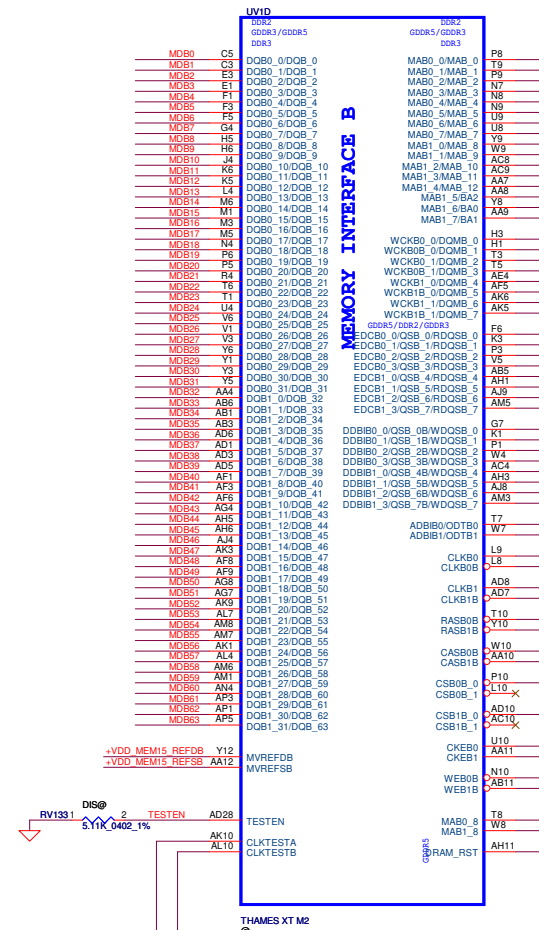
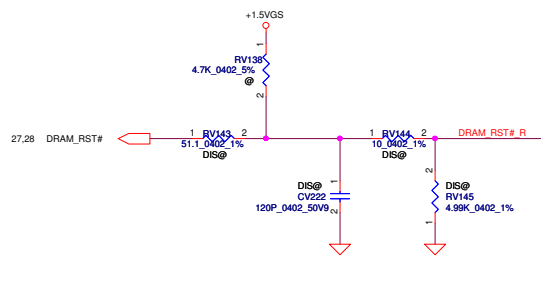
Co-lay Thames/Mars Pro/Chelsea

	Thames M2	Mars Pro	Chelsea M2
RV129	POP	@	@
RV130	@	@	@
RV131	POP	@	@
RV132	@	@	@
RV134	POP	@	@
RV135	POP	@	@
RV206	@	MARS@	@
RV205	@	@	POP

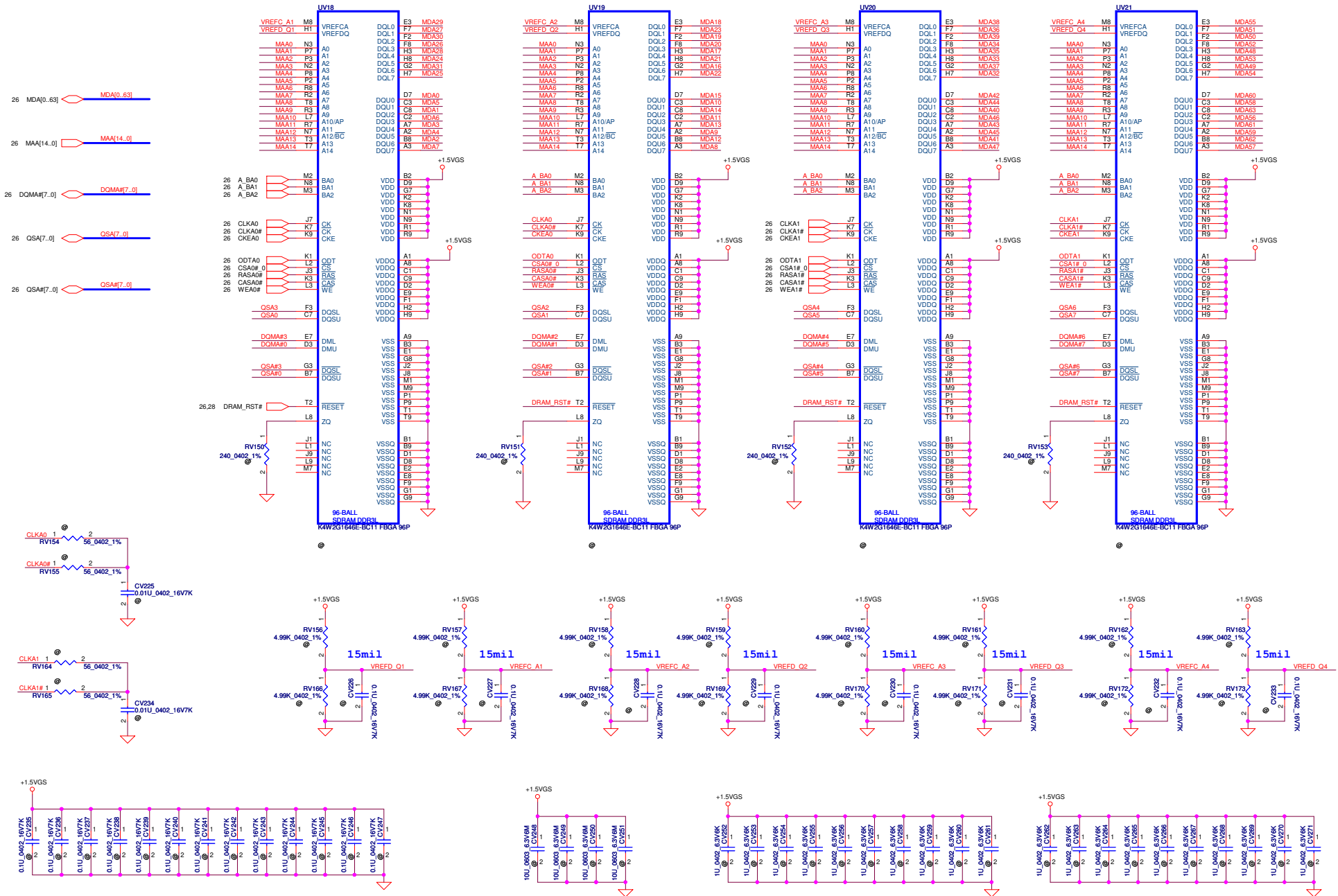


This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and I Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec.

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rsr2

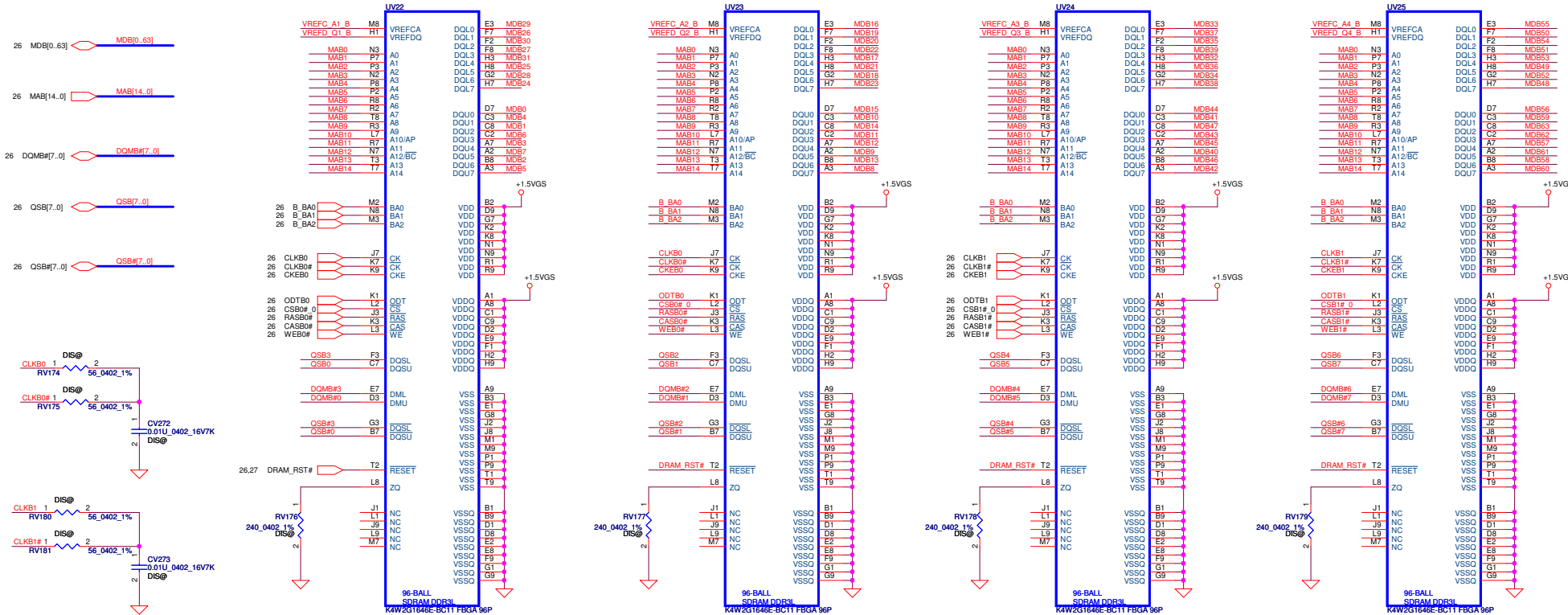


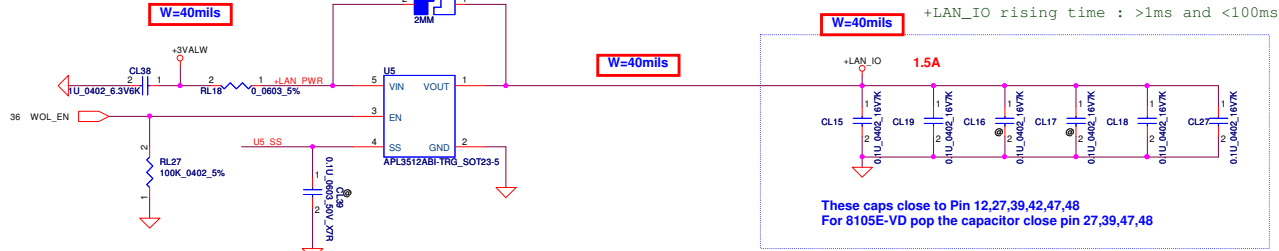
CHANNEL A: 256MB/512MB DDR3



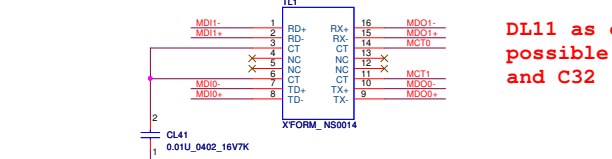
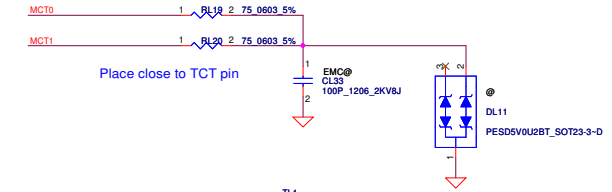
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	ATI ThamesXT M2 VRAM_A
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CHANNEL B: 256MB/512MB DDR3





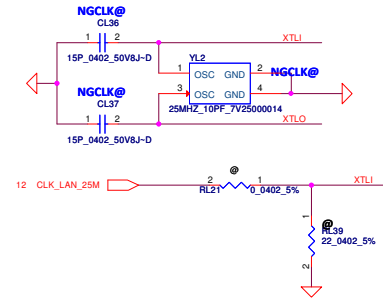
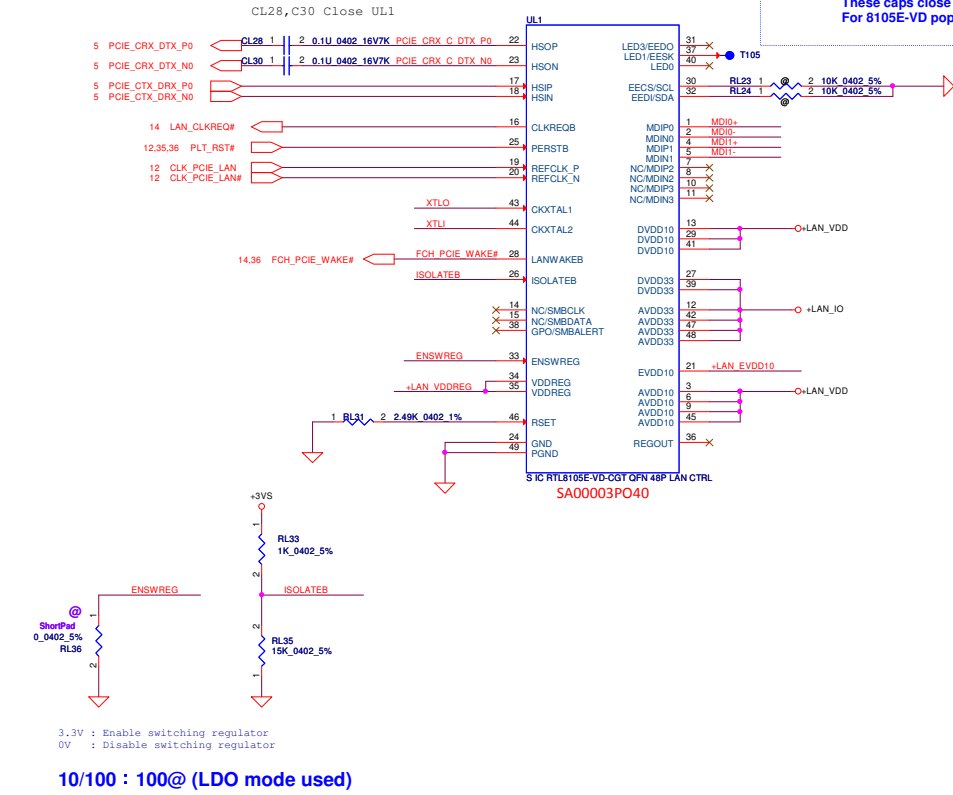
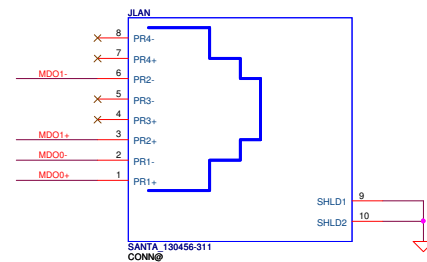
reserve for China Go-rural



Place Close to TL1

reserve for China Go-rural

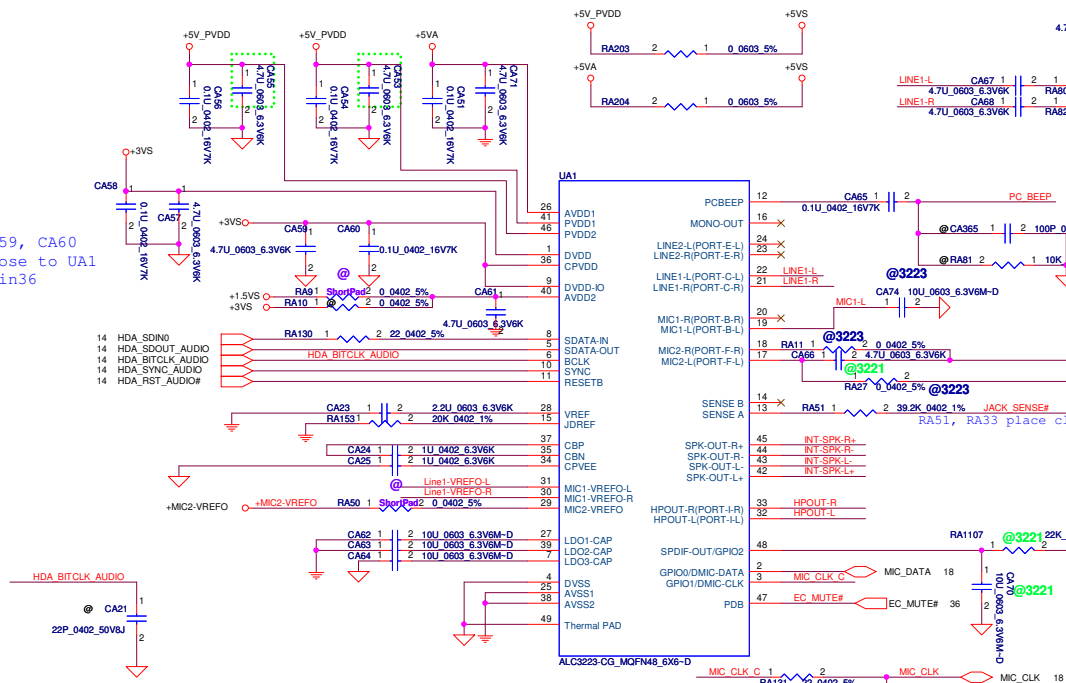
RJ45 Conn.



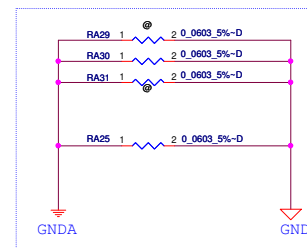
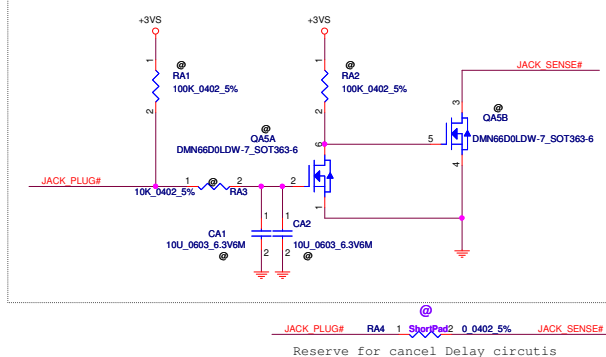
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CA71, CA51 place close to Pin 26

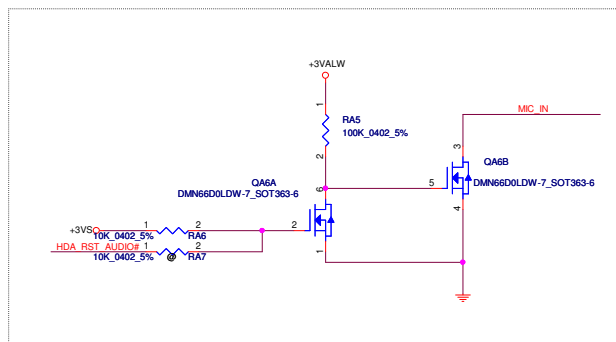
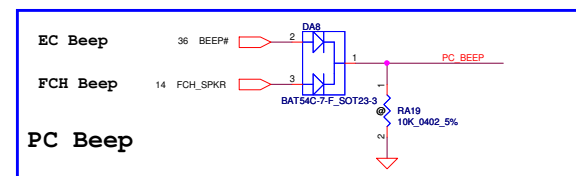
CA59, CA60
Close to UA1
Pin36



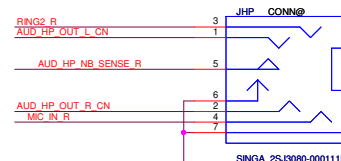
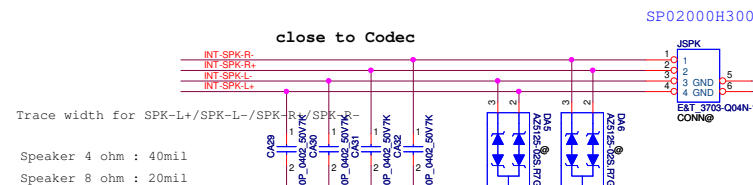
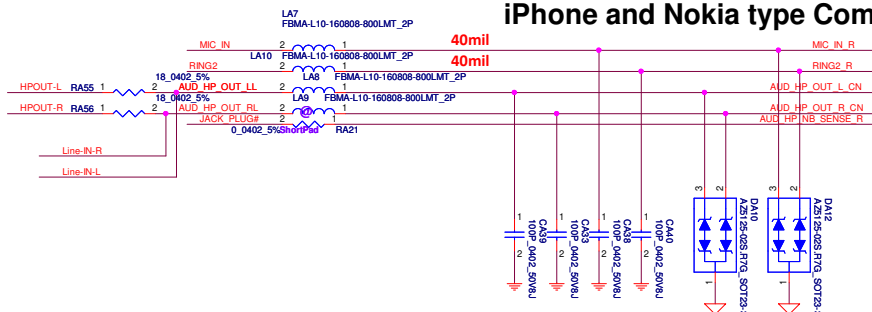
JACK_PLUG Delay circuitis



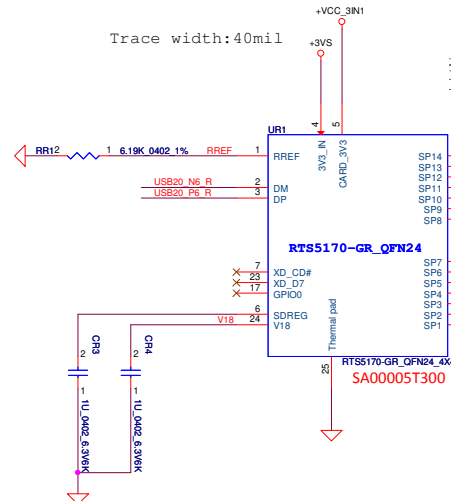
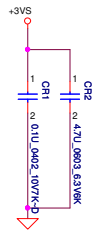
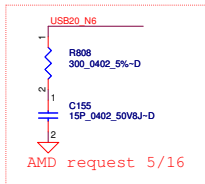
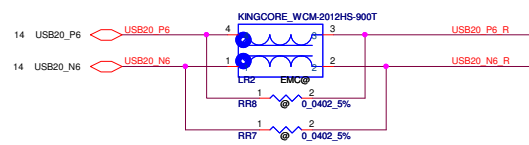
Place on the moat between GND & GND.



iPhone and Nokia type Combo Jack

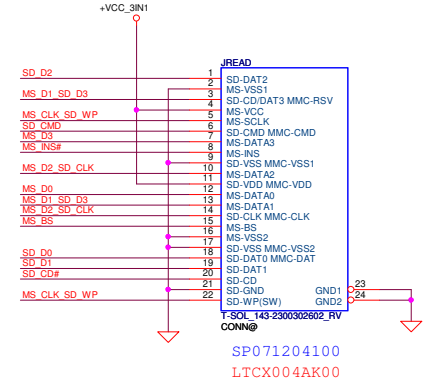
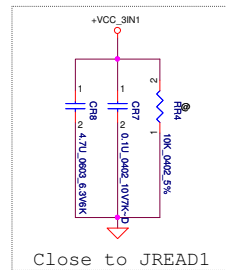
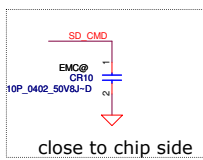
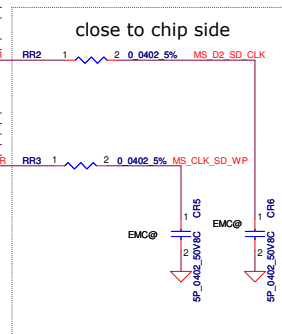


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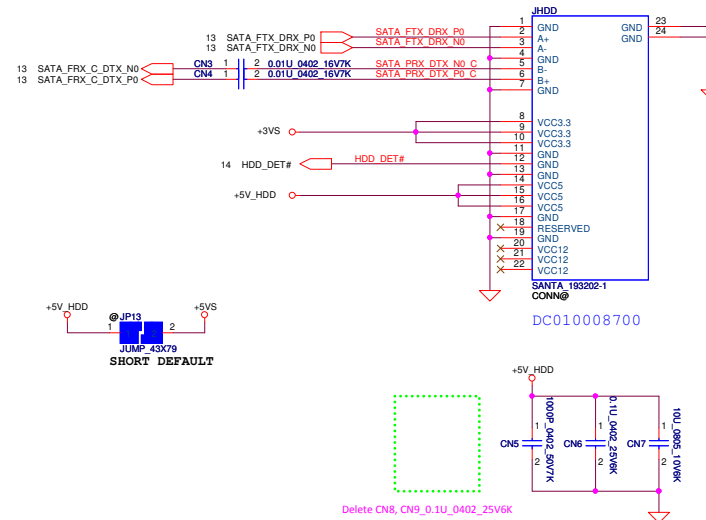
拉MS_D2_SD_CLK到Conn pin 14 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 22 SD_W



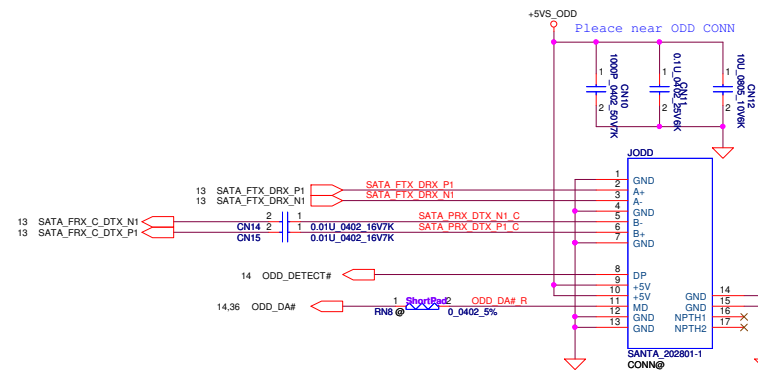
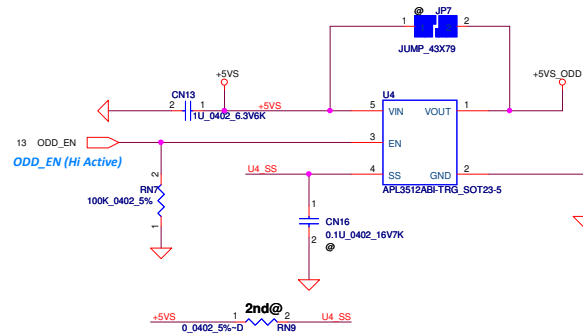
SATA HDD Conn.

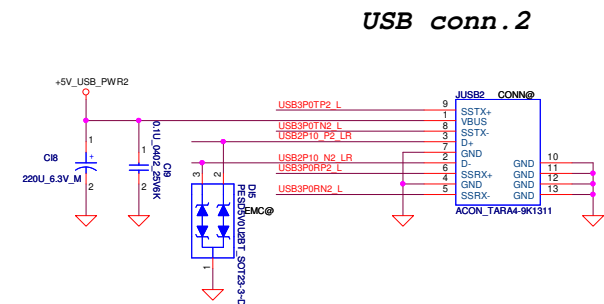
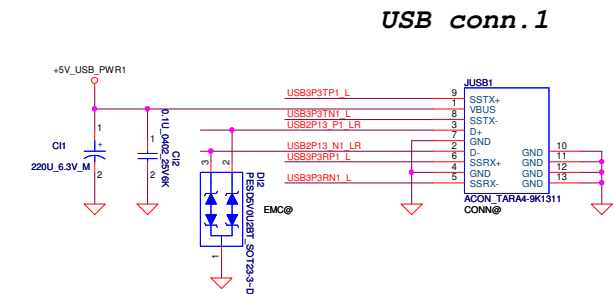
+5V_HDD Source



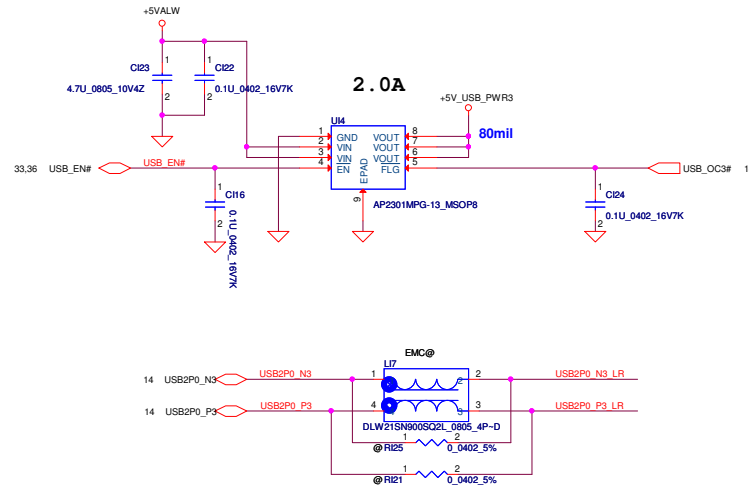
SATA ODD Conn.

ODD Power Control

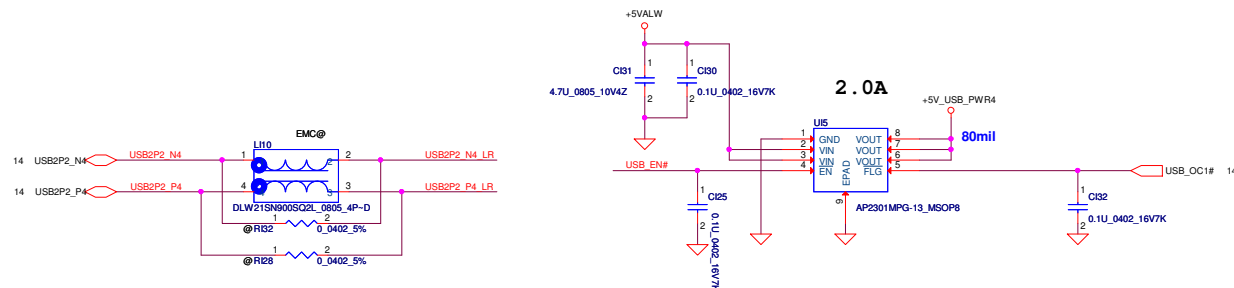
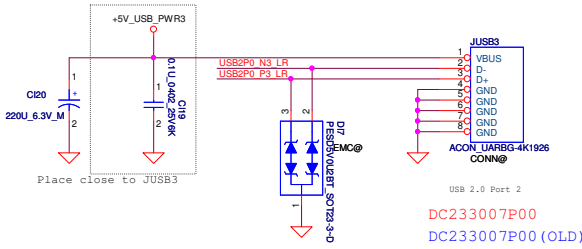




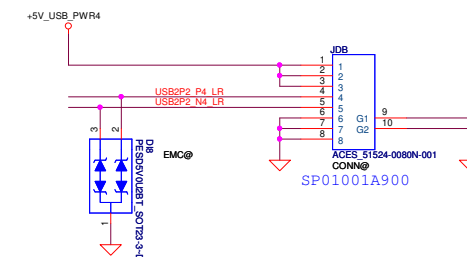
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	USB3.0
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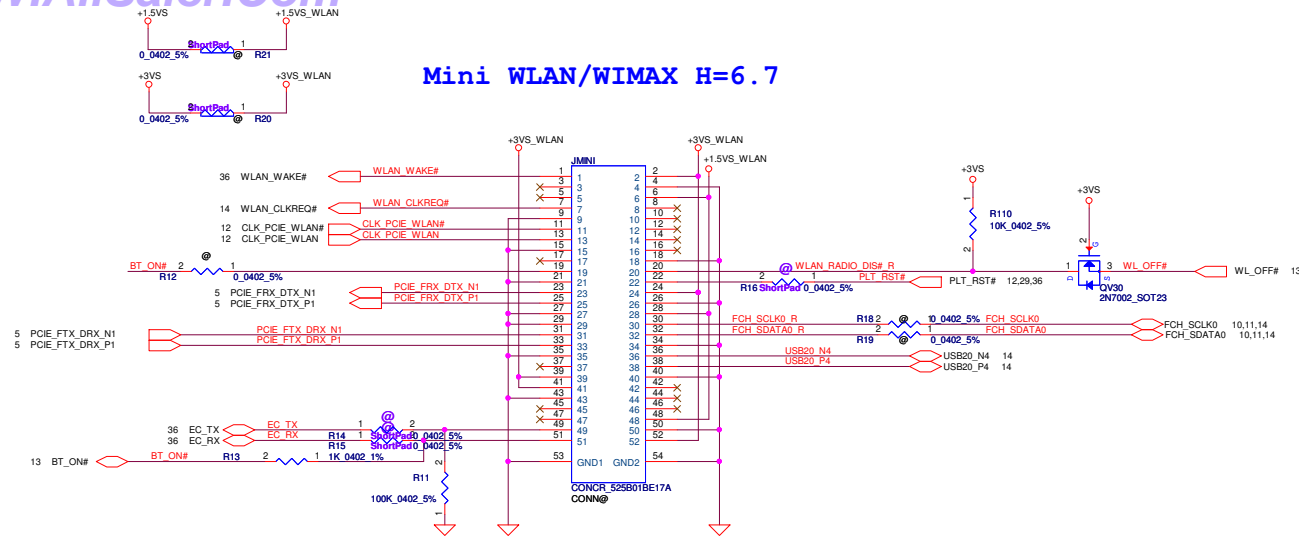
USB conn. 3



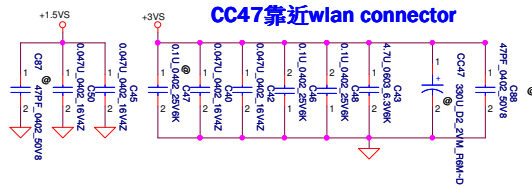
USB conn. 4



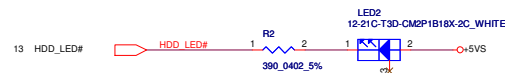
Mini WLAN/WIMAX H=6.7



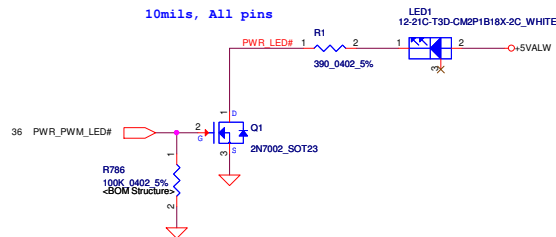
CC47靠近wlan connector



HDD LED



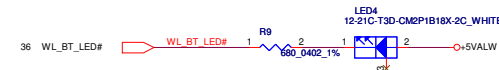
Power LED

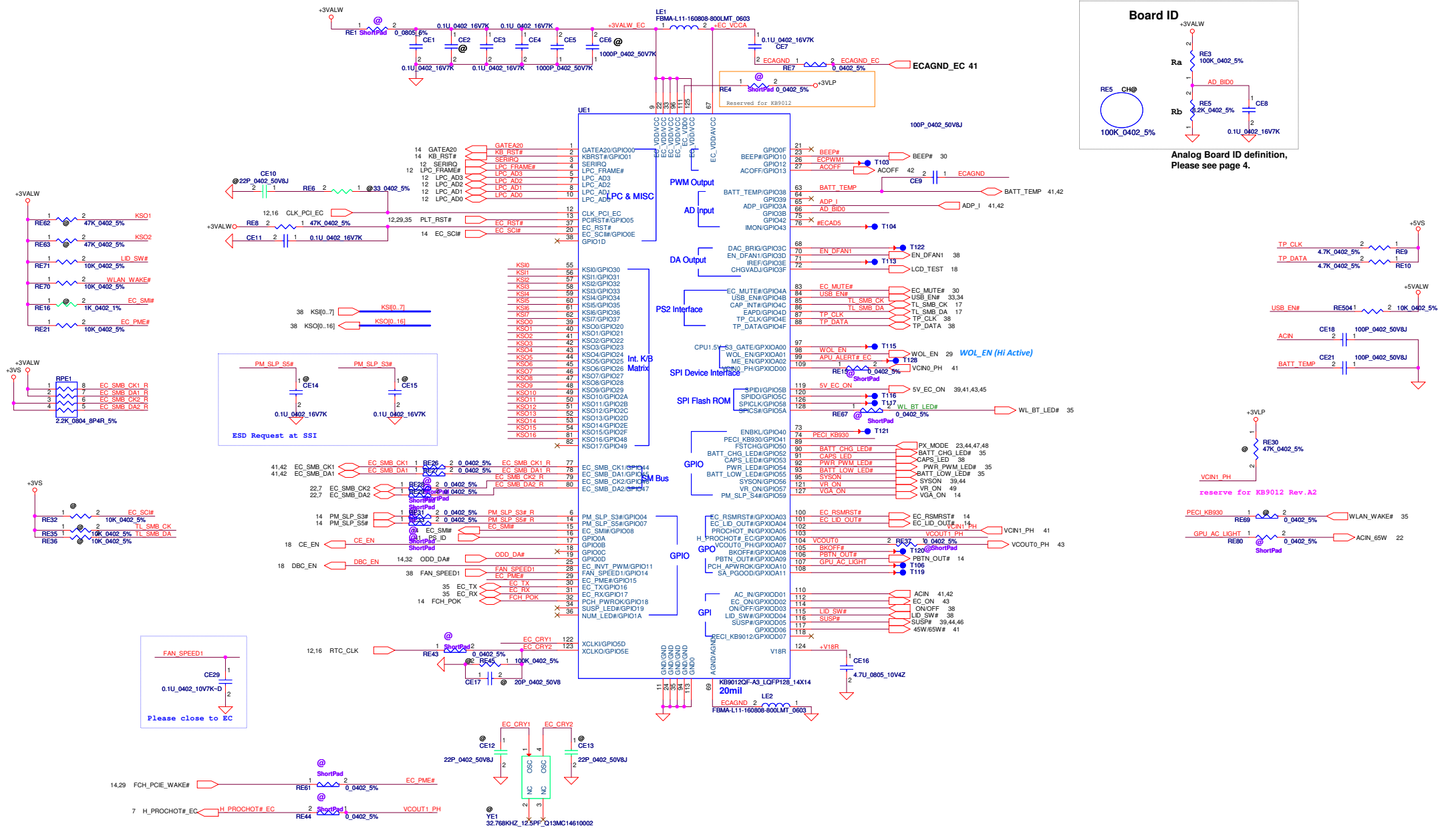


Battery LED

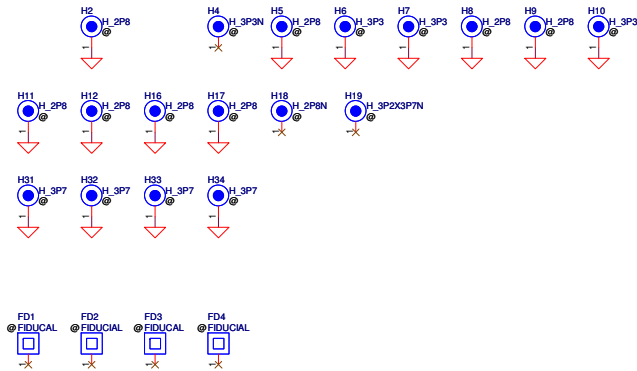


Wireless LED

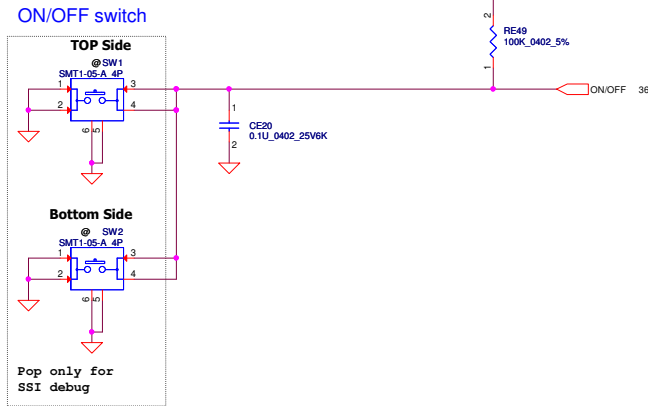




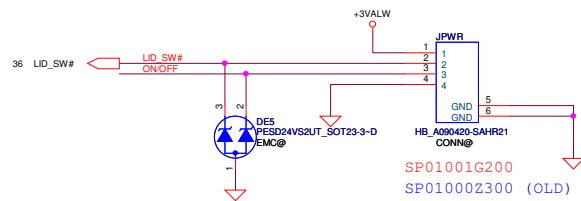
Screw Hole



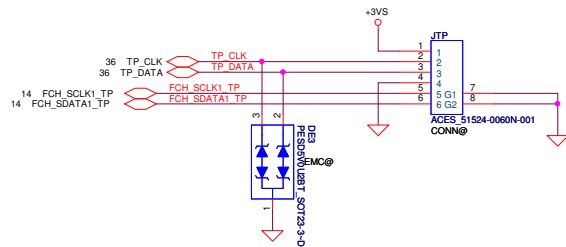
Power ON Circuit



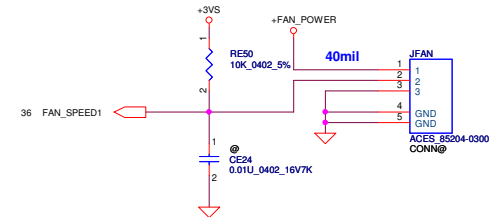
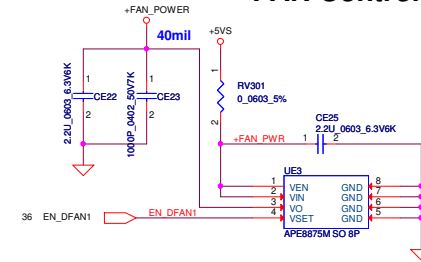
POWER/B



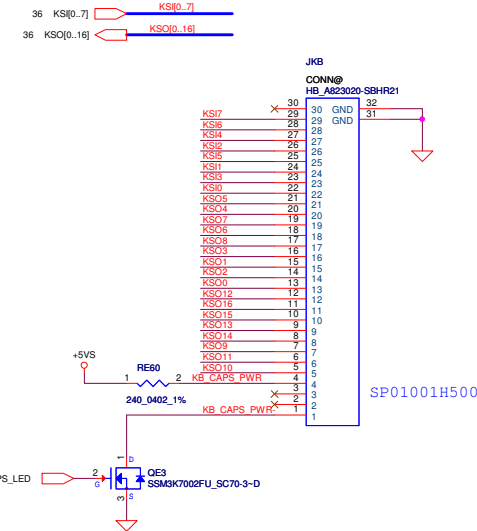
Touch pad

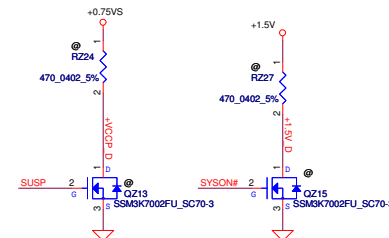
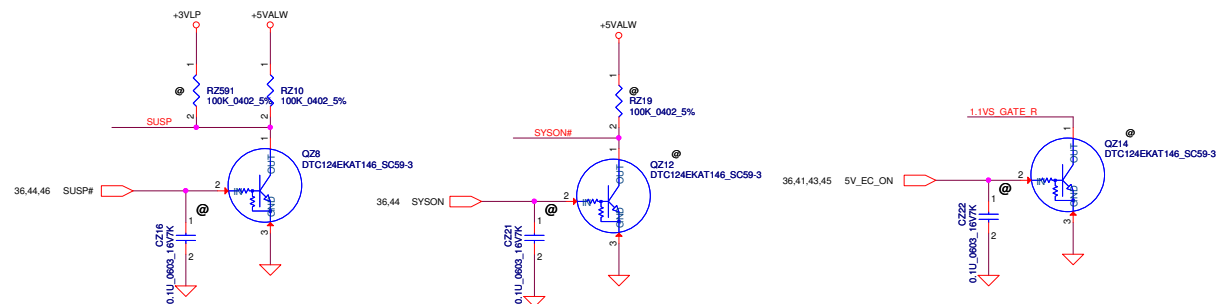
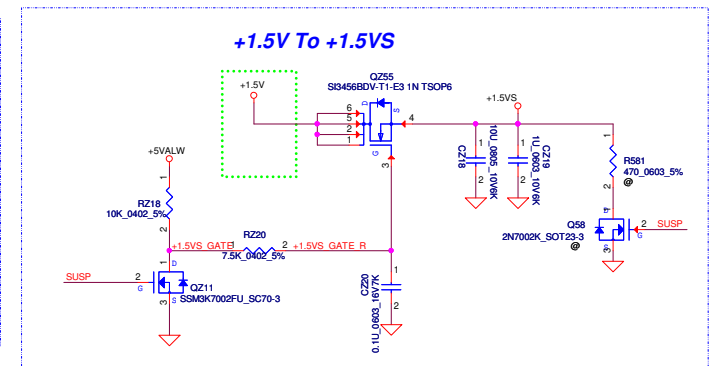
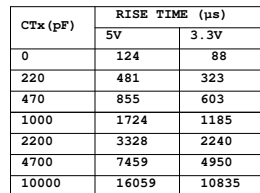


FAN Control circuit



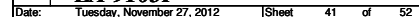
INT_KBD Conn.

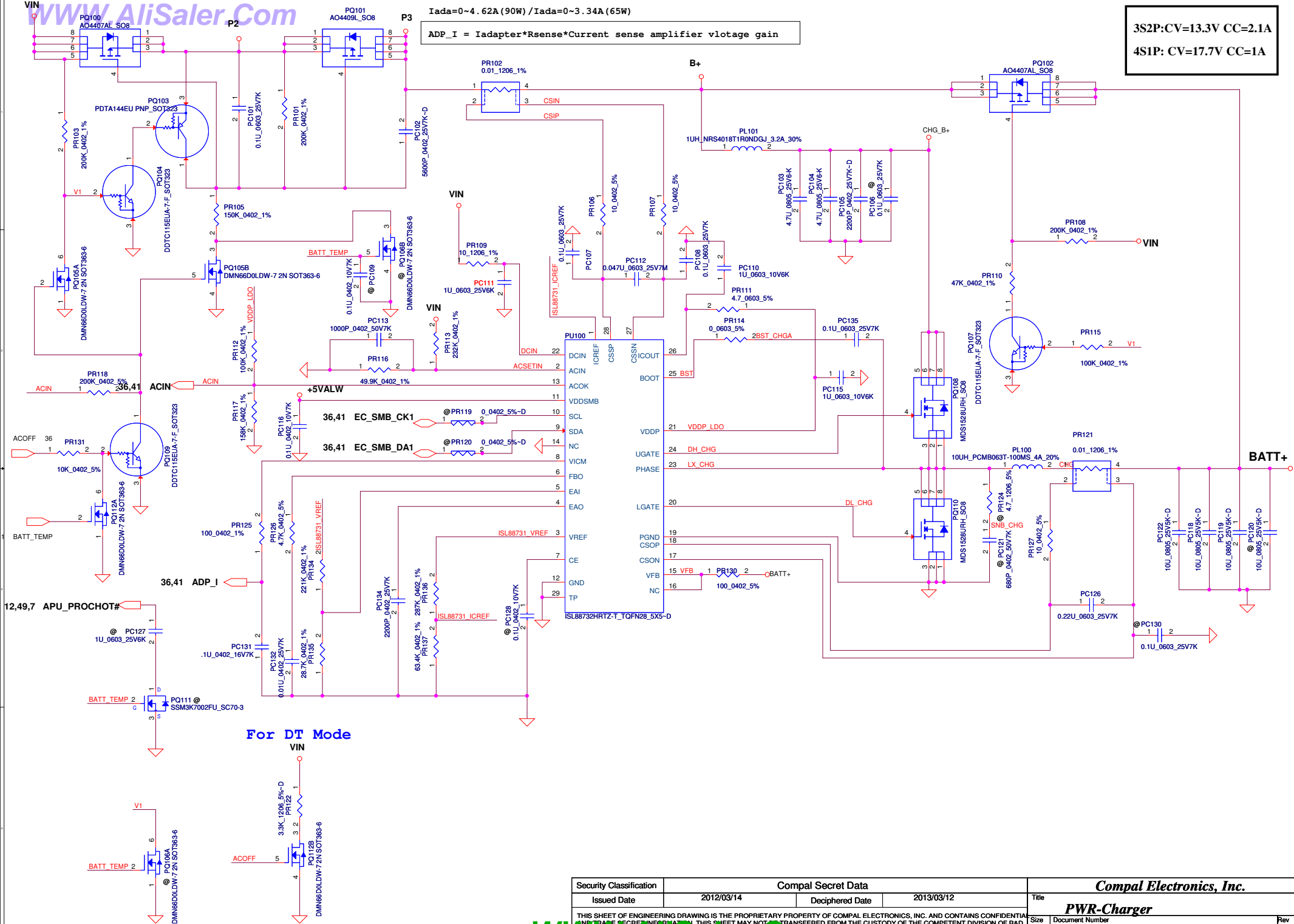




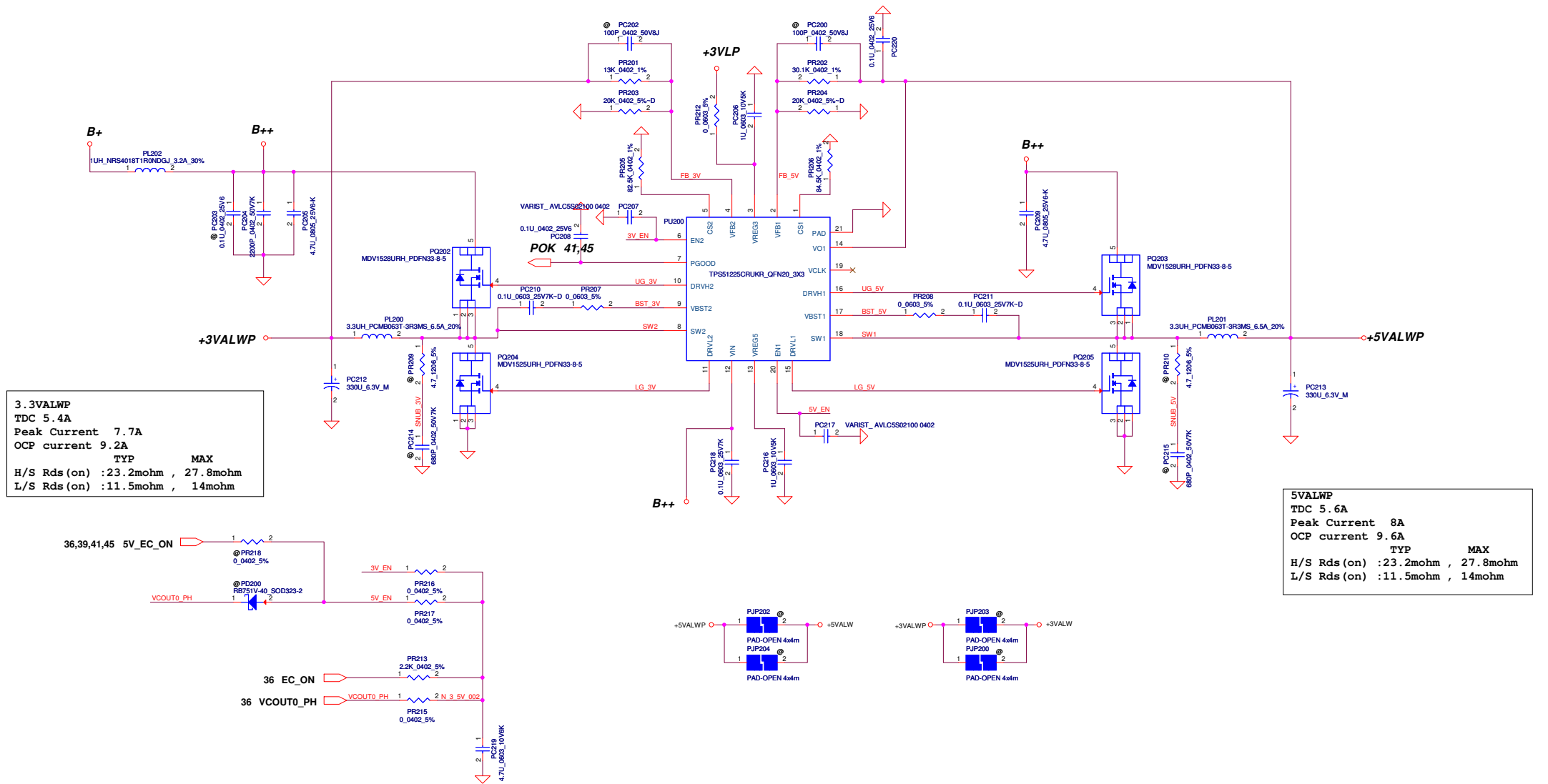
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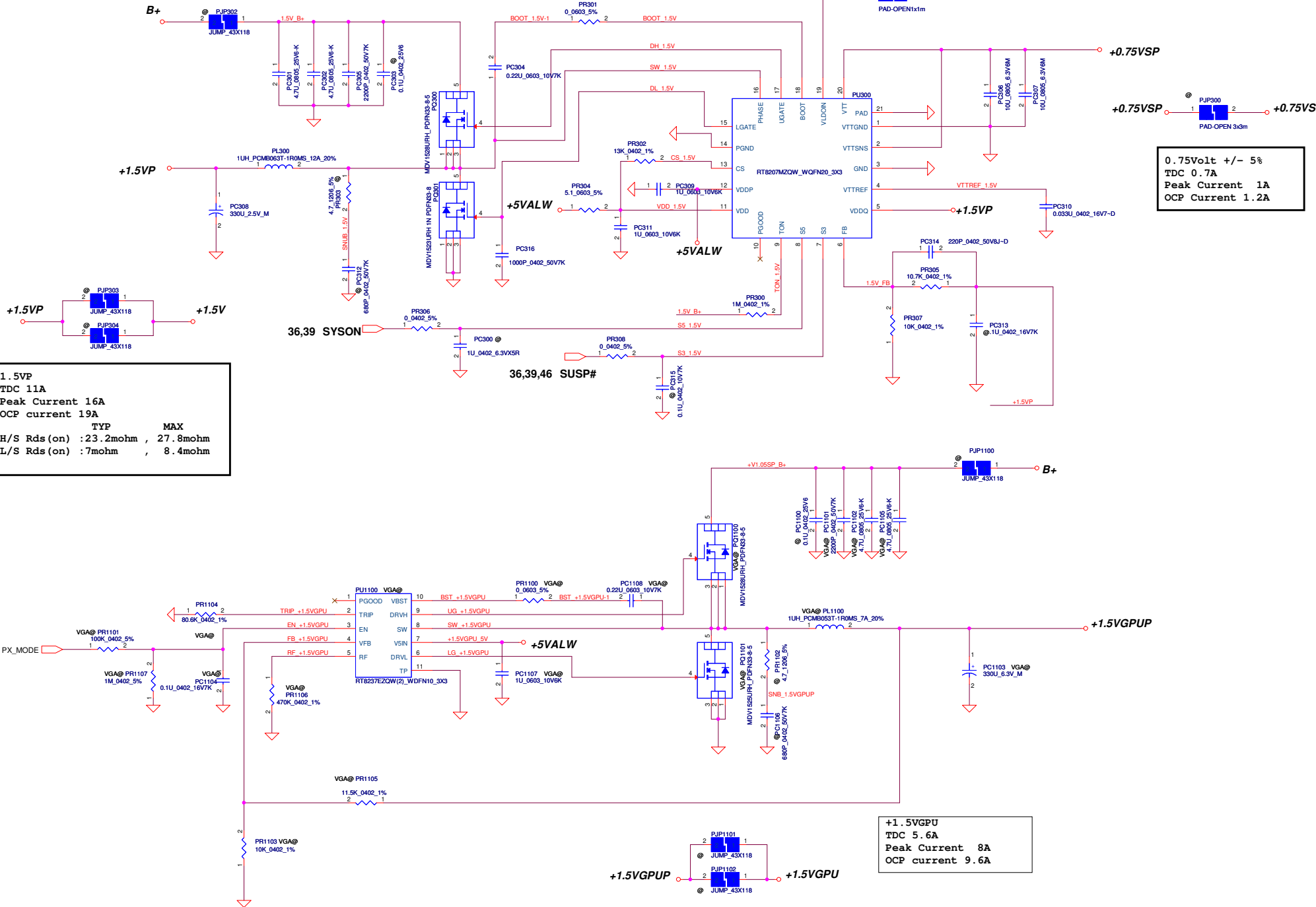
1.





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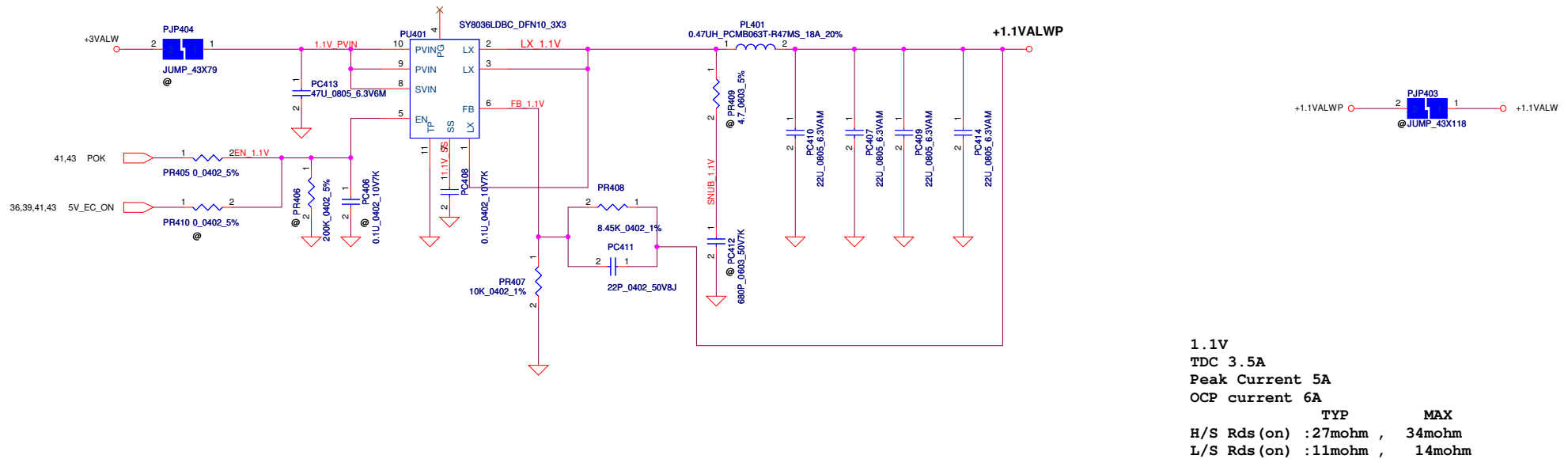
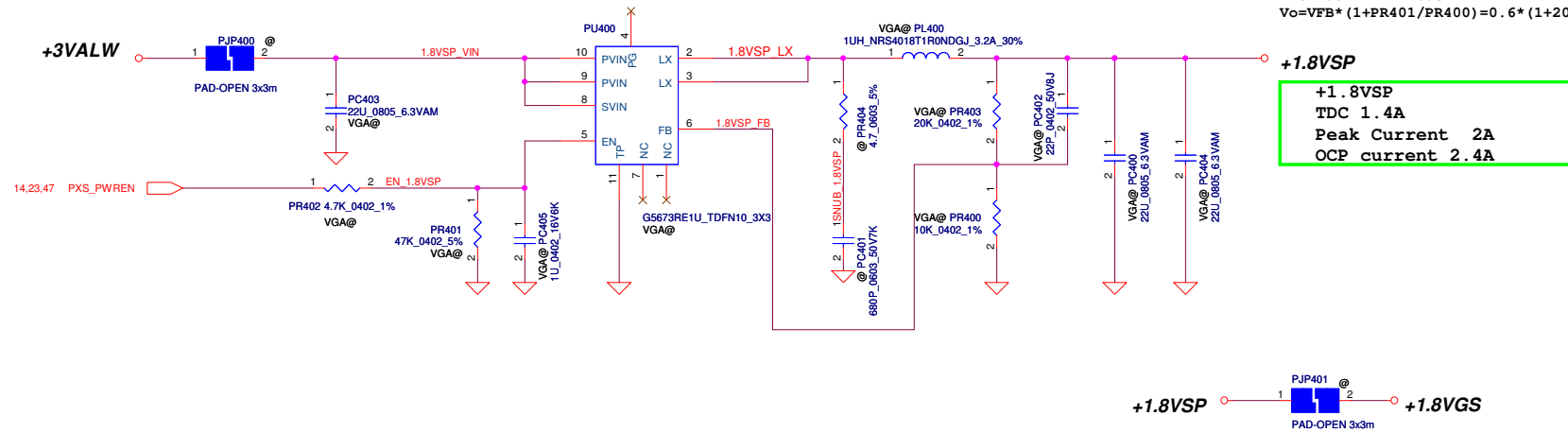


1.5VP
TDC 11A
Peak Current 16A
OCP current 19A
TYP
H/S Rds (on) : 23.2mohm , 27.8mohm
L/S Rds (on) : 7mohm , 8.4mohm

0.75VSP
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

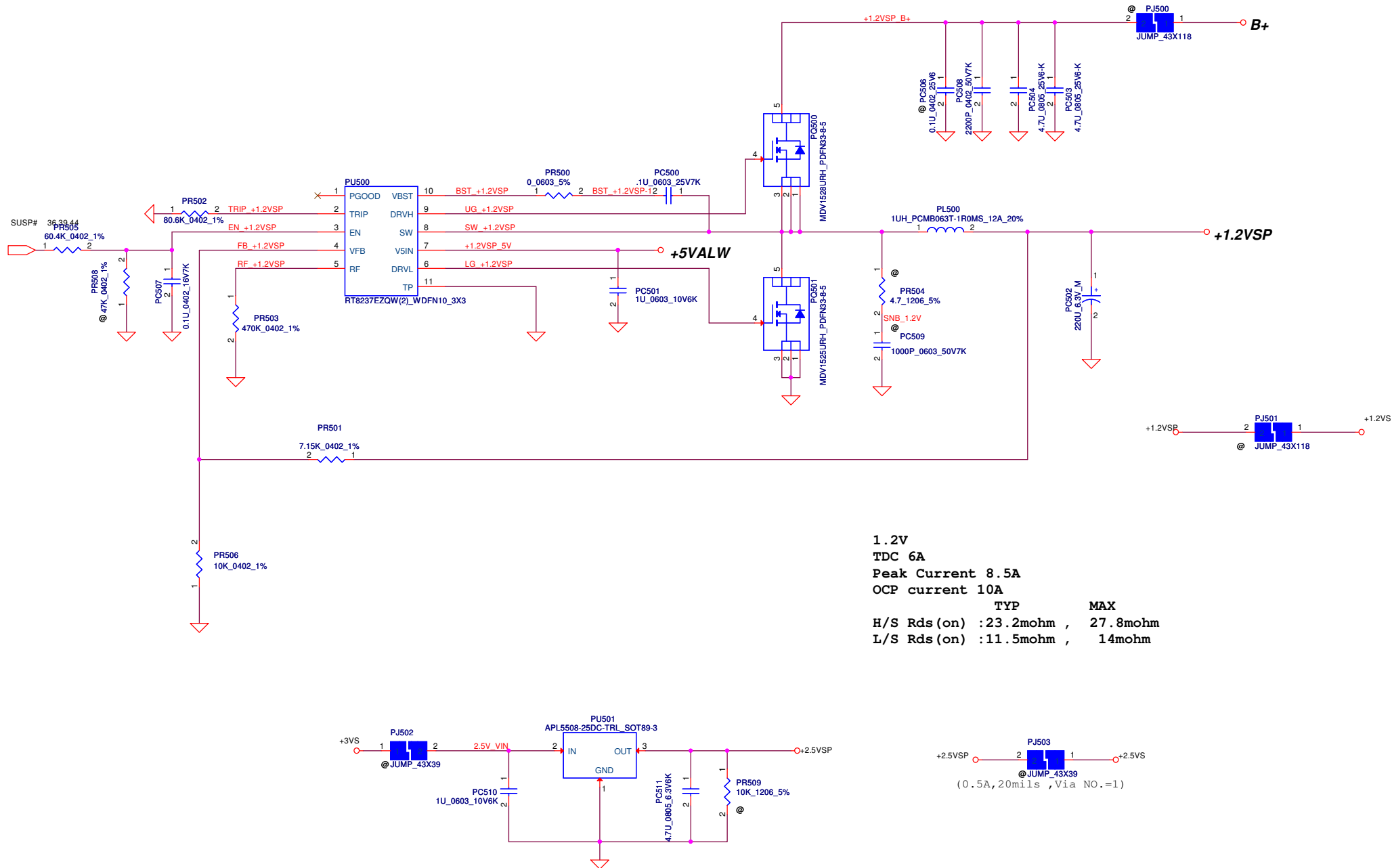
+1.5VGPUP
TDC 5.6A
Peak Current 8A
OCP current 9.6A

<Vo=1.8V> VFB=0.6V
 $V_o = V_{FB} * (1 + PR401 / PR400) = 0.6 * (1 + 20K / 10K) = 1.8V$

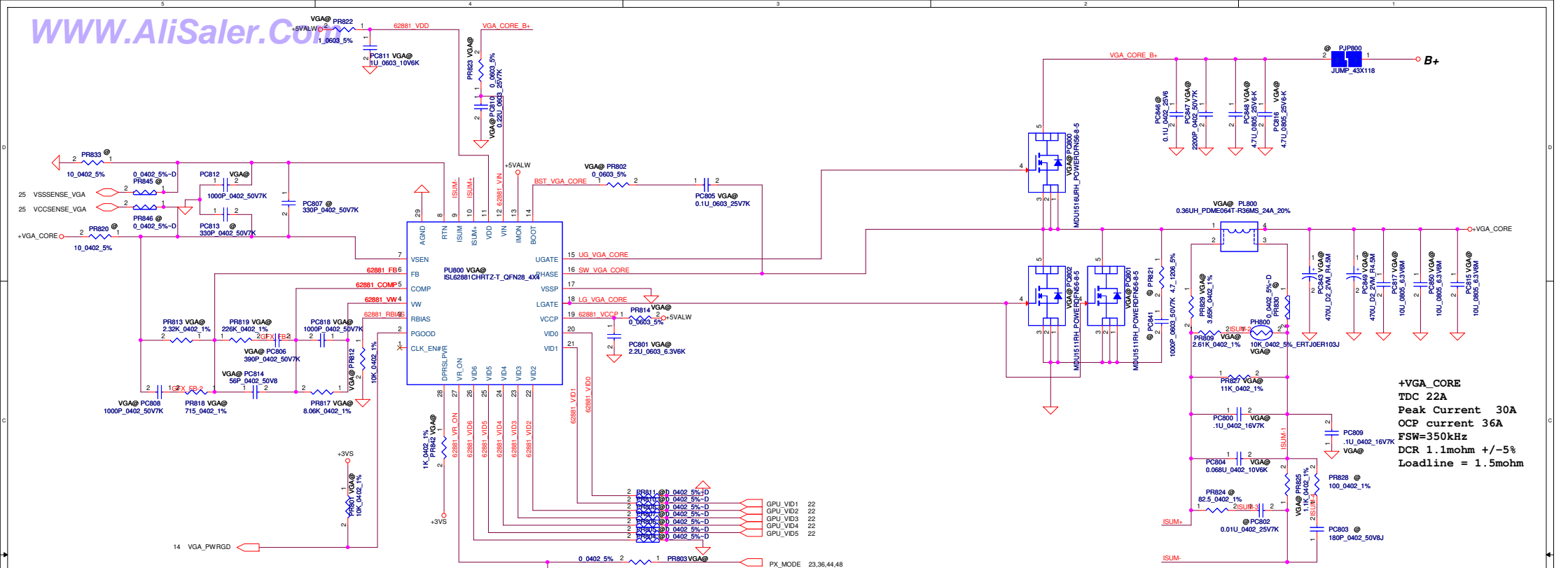


TYP MAX
 H/S Rds(on) : 27mohm , 34mohm
 L/S Rds(on) : 11mohm , 14mohm

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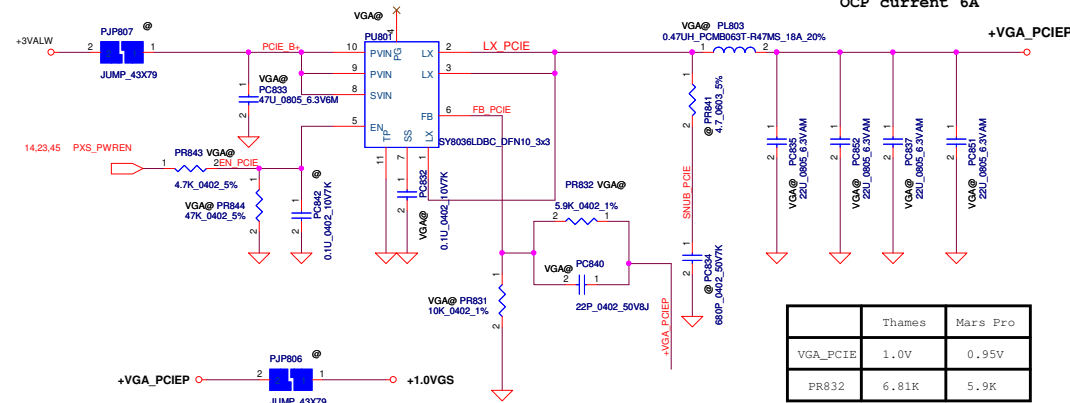
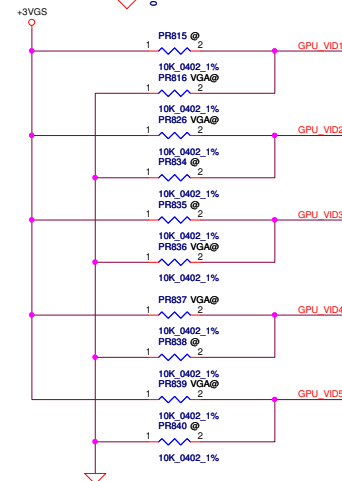


+VGA_CORE
TDC 22A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.1mohm +/-5%
Loadline = 1.5mohm

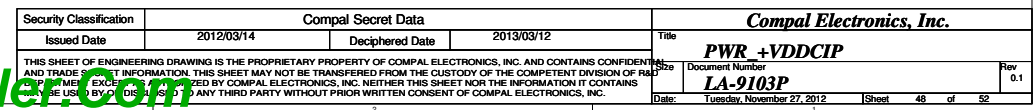
+VGA_PCIE
TDC 3.6A
Peak Current 5.2A
OCP current 6A

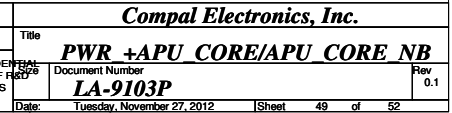
Mars Pro

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	1	0	1	1.025V
1	0	1	0	0	1V
1	0	1	1	0	0.975V
1	0	1	1	1	0.95V
1	1	0	0	0	0.925V
1	1	0	0	1	0.9V
1	1	0	1	0	0.875V
1	1	0	1	1	0.85V
1	1	1	0	0	0.825V
1	1	1	0	1	0.8V
1	1	1	1	0	0.775V



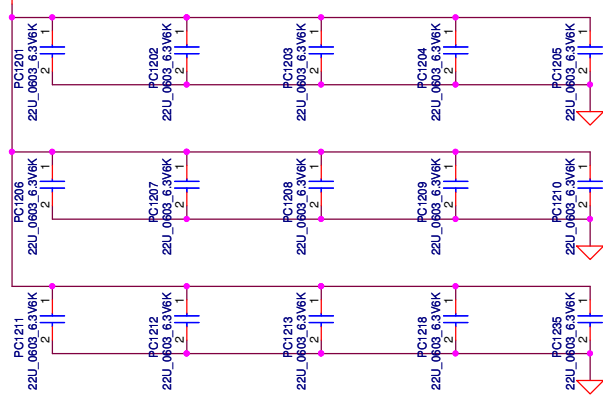
	Thames	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K



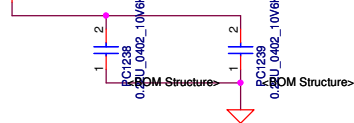


+APU_CORE

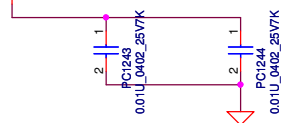
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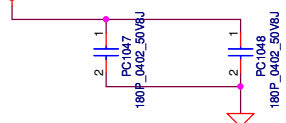
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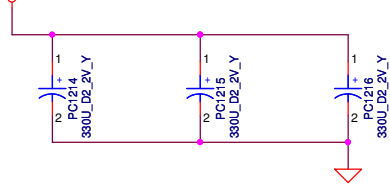
+APU_CORE



+APU_CORE

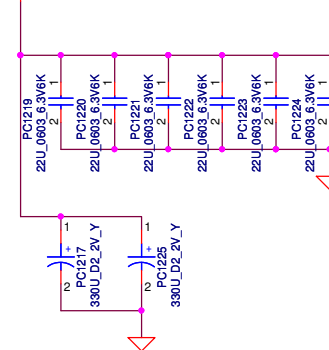


+APU_CORE



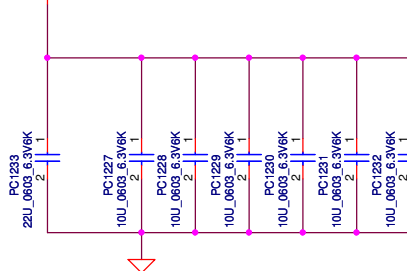
+APU_CORE_NB

+APU_CORE_NB



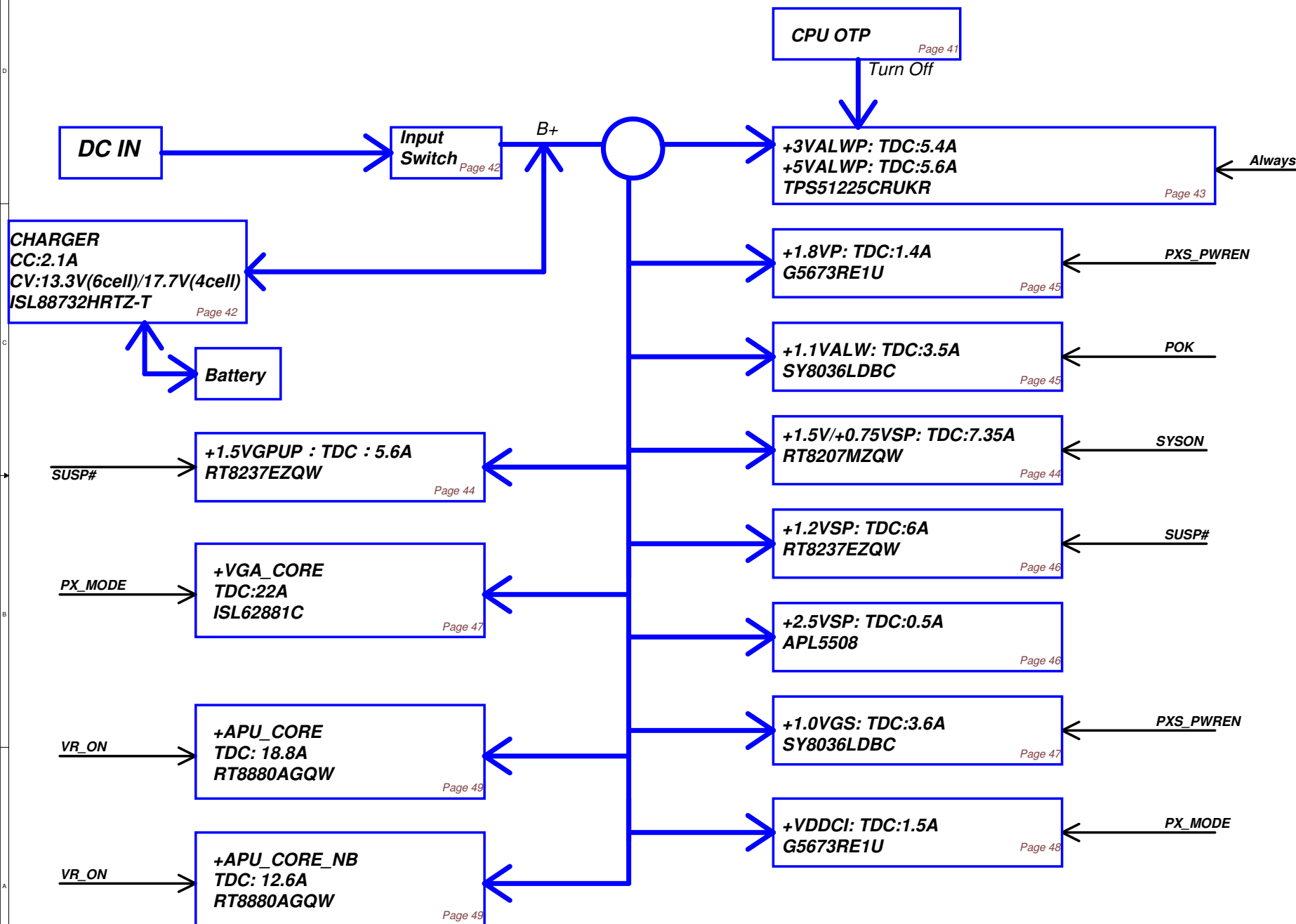
+1.2VS

+1.2VS



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Power block



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